1. Description

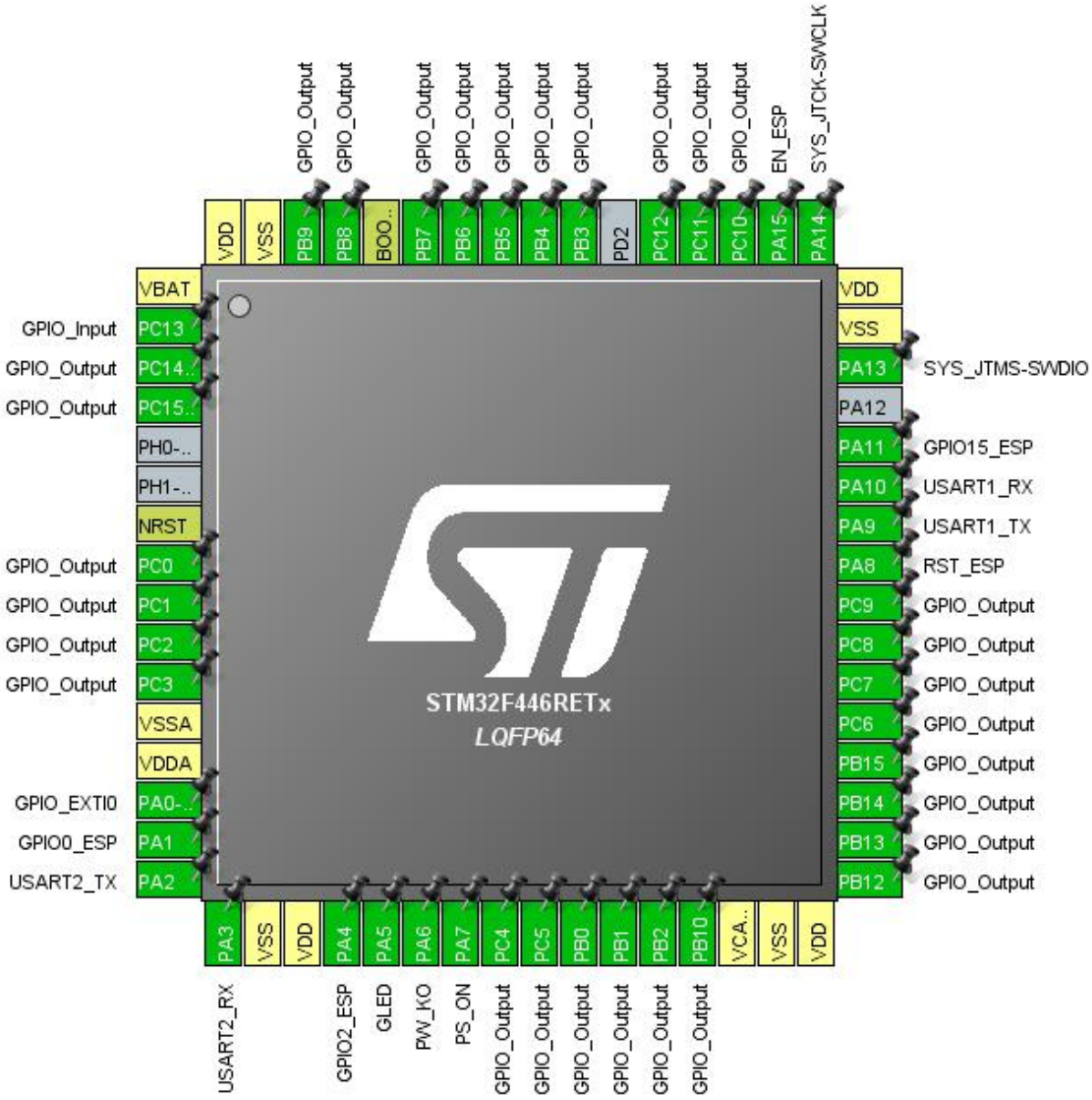
1.1. Project

Project Name	LedTube_CubeMX_Project
Board Name	LedTube_CubeMX_Project
Generated with:	STM32CubeMX 5.0.0
Date	01/23/2019

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



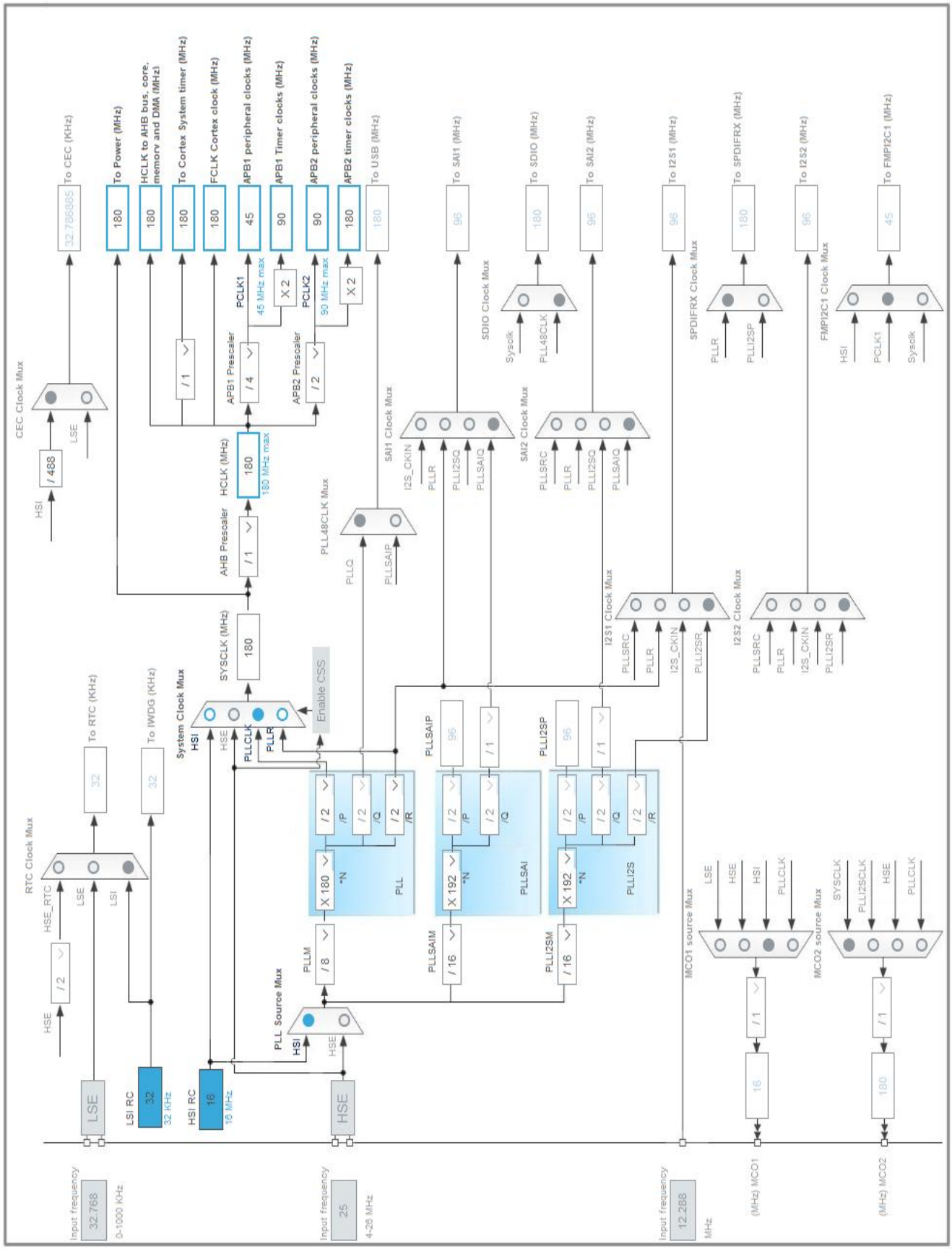
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Input	
3	PC14-OSC32_IN *	I/O	GPIO_Output	
4	PC15-OSC32_OUT *	I/O	GPIO_Output	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Output	
9	PC1 *	I/O	GPIO_Output	
10	PC2 *	I/O	GPIO_Output	
11	PC3 *	I/O	GPIO_Output	
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	GPIO_EXTI0	
15	PA1 *	I/O	GPIO_Output	GPIO0_ESP
16	PA2	I/O	USART2_TX	
17	PA3	I/O	USART2_RX	
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Input	GPIO2_ESP
21	PA5 *	I/O	GPIO_Output	GLED
22	PA6 *	I/O	GPIO_Input	PW_KO
23	PA7 *	I/O	GPIO_Output	PS_ON
24	PC4 *	I/O	GPIO_Output	
25	PC5 *	I/O	GPIO_Output	
26	PB0 *	I/O	GPIO_Output	
27	PB1 *	I/O	GPIO_Output	
28	PB2 *	I/O	GPIO_Output	
29	PB10 *	I/O	GPIO_Output	
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	
34	PB13 *	I/O	GPIO_Output	
35	PB14 *	I/O	GPIO_Output	
36	PB15 *	I/O	GPIO_Output	
37	PC6 *	I/O	GPIO_Output	
38	PC7 *	I/O	GPIO_Output	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
39	PC8 *	I/O	GPIO_Output	
40	PC9 *	I/O	GPIO_Output	
41	PA8 *	I/O	GPIO_Output	RST_ESP
42	PA9	I/O	USART1_TX	
43	PA10	I/O	USART1_RX	
44	PA11 *	I/O	GPIO_Output	GPIO15_ESP
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
50	PA15 *	I/O	GPIO_Output	EN_ESP
51	PC10 *	I/O	GPIO_Output	
52	PC11 *	I/O	GPIO_Output	
53	PC12 *	I/O	GPIO_Output	
55	PB3 *	I/O	GPIO_Output	
56	PB4 *	I/O	GPIO_Output	
57	PB5 *	I/O	GPIO_Output	
58	PB6 *	I/O	GPIO_Output	
59	PB7 *	I/O	GPIO_Output	
60	BOOT0	Boot		
61	PB8 *	I/O	GPIO_Output	
62	PB9 *	I/O	GPIO_Output	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	LedTube_CubeMX_Project
Project Folder	F:\projets\projets2016\electrolab\ledtube\processing\STM32F446RE\code\LedTu
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.9.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes

6. IPs and Middleware Configuration

6.1. SYS

Debug: Serial Wire Debug (SWD)

6.2. TIM2

Clock Source : Internal Clock

6.2.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

6.3. TIM3

Clock Source : Internal Clock

6.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**0xFFFF ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**359 ***
Internal Clock Division (CKD)	**Division by 4 ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

6.4. TIM6

mode: Activated

6.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**9000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**9999 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

6.5. TIM7

mode: Activated

6.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**89 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**0xFFFF ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

6.6. TIM8

Clock Source : Internal Clock

Channel1: Output Compare No Output

Channel3: Output Compare No Output

6.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**71 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Output Compare No Output Channel 1:

Mode	**Toggle on match ***
Pulse (16 bits value)	**20 ***
CH Polarity	High
CH Idle State	Reset

Output Compare No Output Channel 3:

Mode	**Toggle on match ***
Pulse (16 bits value)	**30 ***
CH Polarity	High
CH Idle State	Reset

6.7. USART1

Mode: Asynchronous

6.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

6.8. USART2

Mode: Asynchronous

6.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

7. System Configuration

7.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Fast ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Fast ***	
USART2	PA2	USART2_TX	Alternate Function Push Pull	Pull-up	**Fast ***	
	PA3	USART2_RX	Alternate Function Push Pull	Pull-up	**Fast ***	
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC14-OSC32_IN	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC15-OSC32_OUT	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA0-WKUP	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO0_ESP
	PA4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPIO2_ESP
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GLED
	PA6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PW_KO
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PS_ON
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RST_ESP
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO15_ESP
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EN_ESP
	PC10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

7.2. DMA configuration

DMA request	Stream	Direction	Priority
USART2_TX	DMA1_Stream6	Memory To Peripheral	Low
USART2_RX	DMA1_Stream5	Peripheral To Memory	Low
USART1_RX	DMA2_Stream5	Peripheral To Memory	Low
USART1_TX	DMA2_Stream7	Memory To Peripheral	Low
TIM8_CH3	DMA2_Stream4	Memory To Peripheral	**Very High ***
TIM8_CH1	DMA2_Stream2	Memory To Peripheral	**Very High ***

USART2_TX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_RX: DMA1_Stream5 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_RX: DMA2_Stream5 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA2_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

TIM8_CH3: DMA2_Stream4 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

TIM8_CH1: DMA2_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

7.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
Debug monitor	true	0	0
System tick timer	true	3	0
EXTI line 0 interrupt	true	0	0
DMA1 stream5 global interrupt	true	1	0
DMA1 stream6 global interrupt	true	1	0
TIM3 global interrupt	true	6	0
USART1 global interrupt	true	4	0
USART2 global interrupt	true	4	0
TIM6 global interrupt and DAC1, DAC2 underrun error interrupts	true	5	0
DMA2 stream2 global interrupt	true	0	0
DMA2 stream4 global interrupt	true	0	0
DMA2 stream5 global interrupt	true	1	0
DMA2 stream7 global interrupt	true	1	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM2 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
TIM7 global interrupt	unused		

*** User modified value**

8. Software Pack Report