Si4x6x and EZR32 Low-Power PA Matching

1. Introduction

This application note provides a description of the matching techniques applied to the low-power Si4060 TX, Si4460/61/67, and EZR32 R60/61/67/55 TRX RFIC families. The typical power regime of the Si4461 and EZR32 R61 is in the +13 to +16 dBm range, while the Si4060/Si4460/67 and EZR32 R60/67/55 are primarily devoted to the +10–13 dBm applications.

Specifically, this document does *not* address the matching procedure for the PA on the Si4063/4463/64/68 and EZR32 R63/68 families of RFICs. Because the output power level on the Si4063/4463/64/68 and EZR32 R63/68 families of RFICs is considerably higher than the Si4060/Si4460/61/67 and EZR32 R60/61/67/55 RFIC, the matching procedure is somewhat different.

The matching network achieves a number of goals simultaneously:

- Targets a nominal output power level of +10 to +16 dBm
- Minimizes current consumption (i.e., maximize efficiency)
- Constrains the peak voltage at the drain of the output devices
- Complies with ETSI and FCC specifications for spurious emissions
- Is immune against termination impedance variations as much as possible
- Has low variation over temperature and supply voltage
- Has low bill of materials and cost

Unfortunately, not all of these goals can be satisfied in the most optimal way simultaneously. Silicon Labs investigates different matching types and methods to meet as much as possible with the above requirements. In this document, the best three TX matching types (the switched PA mode Class E (CLE) type, the switched PA mode square wave (SQW) type, and the Switched Current (SWC) type) are presented in detail.

The main advantage of the switched mode (especially CLE) matching types is their very high efficiency. They are proposed for applications where the current consumption is most critical, e.g., the typical total chip current with CLE match (assuming 3.3 V Vdd) is ~17–19 mA at ~10 dBm, ~25 mA at ~13 dBm and ~40 mA at 16 dBm power levels.

The SQW type match is proposed for use only at low frequencies (below 260 MHz, e.g. at 169 MHz), where the Class E operation is not efficient with the Pro IC family due to its low capacitance.

The main disadvantage of the switching type PA matches is the high Vdd dependency (the power variation is proportional to the square of the Vdd change: i.e. dp = ~6 dB in the 1.8–3.8 V range) and the inaccurate nonlinear power steps.

Also their current consumption and the peak voltage on the TX pin are sensitive to the termination impedance variation, and they usually require slightly higher order filtering and thus higher bill of materials cost.

Some of these drawbacks can be cured to varying degrees with special methods that are described detailed later in this document.

The main advantages of the SWC matches are the flat power vs. Vdd characteristic, better stability over temperature, accurate and linear power steps, simpler design process, and lower BOM costs due to the required weaker filtering. Therefore, the SWC match is proposed for applications in which the flat power characteristic and accurate power steps are the primarily concern and where the 10–20% higher current consumption is tolerated.

However, the biggest disadvantage is the significantly worse efficiency compared to class E. Basically, the design can be tuned between better efficiency and better power flatness, i.e., by sacrificing efficiency, better power stability can be achieved.

Typical current consumption of SWC matches tuned for high efficiency (and having worse flatness i.e. dp=~3 dB in the 1.8–3.8 V Vdd range) is 22–23 mA at 10 dBm and 30–32 mA at 13 dBm power levels.

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Typical current of flat power designs (dP=~1 dB in the 1.8–3.3 V Vdd range) is 24–25 mA at 10 dBm and 38 mA at 13 dBm power levels.

Some of the switching type (CLE and SQW) disadvantages mentioned above can be cured to some extent by special methods.

For example, the high V_{DD} variation can be cured efficiently at low power levels (e.g., 10 dBm with Si4060/Si4460/67 or 14 dBm with Si4461), by the so-called adaptive power setting method. Since the low-power matches are usually designed in such a way that the specified power at the specified supply voltage is achieved at a relatively low power level setting, at decreasing supply voltage (e.g., due to a discharging battery), the power drop can be compensated by the proper increase of the power level setting i.e., with the decrease of the switcher loss. Unfortunately, this method works well only at lower power regimes (+10 dBm with Si4060/Si4460/67 and +14 dBm with Si4461) where a low power level setting is enough to get the targeted power, and, thus, there is room for compensation. In these cases, the Class E stability over V_{DD} can be even better than 1 dB in the 3.6–.2.1 V Vdd range.

A low power setting (at low power regimes) with higher switcher loss is also good to have immunity against termination antenna impedance variations. It especially reduces the variation of the dc current consumption with variable environmental conditions suffered by the antenna, which is favorable for long-life battery-operated applications, such as meters or sensors, because the excess current drain is limited.

The operation type (CLE, SQW or SWC) can be set by the PA_MODE (0x2200) register. The 0x18 (Si4060/Si4460/67) and 0x20 (Si4461) values result in switching mode (CLE or SQW) operation, while the 0x19 (Si4060/Si4460/67) and 0x21 (Si4461) values result in SWC operation.

In case of the switched PA mode (SQW and CLE) matches, the power can be set by the DDAC field in the PA_PWR_LVL (0x2201) register. The DDAC determines the number of used switching MOS fingers and thus the on-state resistance of the switcher.

In the case of SWC operation, the PA behaves like a high-impedance switched current generator; so, besides the number of fingers (DDAC), the delivered current per finger also determines the power. The current delivered by a finger can be set by the OB field of the PA_BIAS_CLKDUTY register in 10 µA steps.

Here, it is important to note that the critical output parasitic cap value of the PA does not depend on the number of active fingers (DDAC) as determined by the uppermost cascode MOS device connected to the TX pin.

It is theoretically possible to increase the efficiency of low-power CLE matches by reducing the current of the internal PA drivers. For that, they can work in 25% duty cycle mode, by setting all bits of the CLK_DUTY field in the PA_BIAS_CLKDUTY register (0x2202) to 1, resulting in a PA_BIAS_CLKDUTY register value of 0xC0.

The 10 dBm and 13 dBm CLE matches with Si4060/Si4460 use this 25% duty cycler mode to save current. The drawback of this mode is the increased harmonic content and the consequently greater number of filtering components.

With 50% duty cycle mode (PA_BIAS_CLKDUTY register is left in its default value of 0x00), the Si4060/Si4460/67 high power (HP) CLE matches can achieve the 13–14 dBm power with sufficient margin, even with multilayer inductors. However, in this case, the current consumption will be nearly the same as it is with the Si4461 matches. Since the Si4461 has more robust PA, which is designed primarily to the 13–14 dBm power range, there is no reason to use the Si4060/4460/67 ICs instead in 50% duty cycle CLE mode.

The matching procedure outlined in this document for CLE/SQW and SWC allows the user to achieve the above mentioned properties and is applicable for two different types of board configurations: one with separate antennas for the TX and RX paths (Split TX/RX board configuration: in the case of TX only chips (Si4060) the TX path can be used by simply omitting the RX path) and one with a single antenna where the TX and RX paths are tied directly together without the use of an RF switch (Direct Tie board configuration: again, in case of TX only chips (Si4060), the TX path can be used and the Rx path can be omitted).

The differences in the matching procedure required for the two board configurations are discussed in detail.

The next chapter is provided for users more interested in quickly obtaining matching component values than in the methodology used to develop the matching network. The methodology is described in detail in Sections 3, 4, and 5.

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Table 1. Silicon Labs EZRadio Pro Sub-GHz Wireless IC Family RF Match Cross References

Match Type	Advantages	Disadvantages	RF IC Types						
			Si4463/64/68 (TRX)	Si4461 (TRX)	Si4460/67 (TRX)	Si4438 (TRX)	Si4063 (TX)	Si4060 (TX)	Si4362 (RX)
Class E Split	High Efficiency, High Power	power varies with VDD, nonlinear power steps	AN648, 868/915M 20 dBm & 85 mA	AN627, 434/868M 13–16 dBm & 26–43 mA	AN627, 434/868/ 915M 10…13 dBm & 16–24 mA	AN732, 490 MHz, 20 dBm & 85 mA	AN648, 868/915M 20 dBm & 85 mA	AN627, 434/868/915M 10–13 dBm & 16–24 mA	—
Class E DT	High Efficiency, High power, One antenna	power varies with VDD, nonlinear power steps	AN648, 868/915M 20 dBm & 85 mA	AN627, 434/868M 13–16 dBm & 26.5–43 mA	AN627, 434/868/ 915M 10–13 dBm & 17–25 mA	AN732, 490 MHz, 20 dBm & 85 mA	—	—	—
Class E TX/RX Switch	High Efficiency, One antenna	power varies with VDD, nonlinear power steps, extra RF switch adds cost	AN648, 868/915M 20 dBm & 85 mA	—	—	—	—	—	—
SQW DT	High Efficiency, High power, one antenna	power varies with VDD, nonlinear power steps	AN648, 169M 20 dBm & 70 mA	—	AN627, 169M, 10 dBm & 18 mA	—	—	—	—
SWC SPLIT	Flat VDD characteristic, lower BOM (than class E), linear power steps	less efficient, medium power	—	AN627, 868/915M 13–14 dBm & 31–36 mA	AN627, 315/ 434/868/ 915M 10 dBm & 24 mA	—	—	AN627, 315/434/868/ 915M 10 dBm & 24 mA	—
SWC DT	Flat VDD characteristic, lower BOM (than class E), linear power steps, one antenna	less efficient, medium power	—	AN627, 868/915M 13–14 dBm & 31–36 mA	AN627, 315/434/868/ 915M 10 dBm & 24 mA	—	—	—	—
4 Element RX Match	Balun with minimum phase and magnitude error, fully matched		—	—	—	—	—	—	AN643, 10/13 mA

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2. Summary of Matching Network Component Values

Some users are not greatly interested in the theoretical development of the matching network; rather, they are concerned with quickly obtaining a set of component values for a given desired frequency of operation. For those users, the resulting component values for the CLE, SQW and SWC PA matching network for multiple frequencies and power levels across the operating range of the Si4060/Si4460/67 and Si4461 RFIC are summarized in this section.

The radio cores of the EZR32 R60/67/55 and R61 wireless MCUs are based on the Si4460 and Si4461 RFICs, respectively, so basically the same matching networks can be used for them. However, slight element value modifications might be required due to the different chip package, i.e., different on-chip parasitic capacitances and bonding wire inductances between Si446x and EZR32. Additionally, Silicon Labs' EZR32-based reference designs typically use more-layer PCBs than the Si446x-based reference designs, so the PCB parasitics are also different. In some cases, especially at the higher frequency bands, this may cause slightly different tuned component values in the matching network between the Si446x- and EZR32-based reference designs despite the same radio core inside.

By default, the same matching network element values should be used for both EZRadioPRO Si446x RFICs and EZR32 wireless MCUs, otherwise noted in the document where the EZR32-based design should use slightly different tuned component values from the relevant Si446x-based network.

The matching networks may be realized with either wire-wound SMD inductors or multi-layer SMD inductors. The cost of a multi-layer inductor is significantly lower than that of a wire-wound inductor, and, thus, in cost sensitive applications, the multi-layer solution is preferred. However, the performance of a circuit realization using only wire-wound inductors is generally better due to the higher Qs and lower ohmic losses than multi-layer inductors of equivalent value. Due to the increased loss, a realization using multi-layer inductors typically requires a higher power level setting and thus exhibits a slight increase in current consumption for the same amount of output power.

Also, multi-layer SMD inductors are often available only in coarser-spaced inductance values. It may cause a higher deviation from the ideal class E values, especially in Direct Tie solutions where significant adjustments of the value of L0 are usually necessary in order to avoid degradation to RX sensitivity; this may be more difficult with only the set of values available for a multi-layer series of inductors.

The component values shown in these tables are appropriate for a supply voltage of V_{DD} = 3.3 V.

For other V_{DD} voltages the 10 dBm Si4060/Si4460/67 and 14 dBm Si4461 CLE design needs adjustment of the PA power level (e.g., the previously-mentioned adaptive power control), which, to some extent, can compensate the power variations. However, in case of 13–14 dBm Si4060/Si4460/67 and 16 dBm Si4461 CLE designs, the power setting is close to maximum, and, thus, the margin for power degradation compensation at low supply voltage levels is very limited.

The output power of a properly-matched SwC PA is relatively insensitive to the supply voltage changes; so, the component values and the power level settings (DDAC and OB register fields) can be used for other values of V_{DD} as well.

The matching networks are separated based on RFIC (Si4060/Si4460/67 and Si4461) types due to the different PA properties.

The Si4461 PA has 127 MOS switching fingers so the DDAC register can go up to 0x7F. Its typical output capacitance is 2.0 pF independently of the DDAC setting due to its cascade architecture.

The Si4060/Si4460/67 PA has 79 MOS switching fingers; so, the DDAC register can go up to 0x4F. Its typical output capacitance is 1.25 pF independently of the DDAC setting due to its cascade architecture.

The component values shown in the following sections are appropriate when using 0402-size SMD components, such as the 0402HP-series of wire-wound inductors from CoilCraft, the LQG15HS-series of multi-layer inductors from Murata, and the GRM15-series of ceramic capacitors from Murata. These values are appropriate for use on the official Split TX/RX and Direct Tie reference board designs available on the Silicon Labs web site. The presented solutions are likely to operate satisfactorily with 0603-size SMD elements as well.

Surface-mount 0603-size or 0402-size components contain parasitic elements that modify their effective values at the frequency of interest. Furthermore, it is convenient to use the nearest-available 5% or 10% component values rather than the exact component values predicted by, for example, filter design CAD software or filter prototype

tables. Additionally, any printed circuit board layout has parasitics, such as trace inductance, component pad capacitance, etc. These parasitics also depend on the board layout stack-up, i.e., number of layers.

This means that it will almost certainly be necessary to adjust the final matching values for the reader's specific application and board layout. The above component values should be used as starting points and the values modified slightly to zero-in on the best filter response and impedance match to 50 Ω.

2.1. Component Values for Si4461/EZR32 R61 Matching

The Si4461 High Efficient SWC and CLE matches fit most for the 13–14 dBm power regime. At this power level, the CLE has enough margin to be stable over V_{DD} with adaptive power control. The basic 13–14 dBm Si4461 SWC match is optimized for efficiency around 3.3 V. Despite, the power drop in the 1.8–3.6 V Vdd range is only 2–3 dB, much better than that of the CLE match. It has also linear power steps.

A second 868M SWC match optimized for flat power characteristic (dP=~1 dB) is also given in the tables below, but with higher current consumption.

The efficiency of the CLE solution is still significantly better than that of any SWC solution.

The 16 dBm regime can be achieved only with CLE matching. Unfortunately, as mentioned previously, it has high variation over supply voltage because adaptive power control is no longer efficient due to the power setting here, which is close to the maximum.

2.1.1. Si4461 with Split TX\RX SWC Board Configuration: Component Values and Performance

Table 2 provides the component values required for output power levels of both +13 and +14 dBm, using the Split SWC TX/RX board configuration of Figure 1 and a supply voltage of V_{DD} = 3.3 V. The matches described in Table 2 are optimized for the best efficiency and use wire-wound type inductors. At the time of this writing, no Si4461 SWC split match with multilayer inductors are fully tested, but the matches given in Table 2 give satisfactory results with multilayer inductors as well (if an inductor value does not exist, use the closest one). Some tuning (slight increase on OB and/or DDAC value) of the power setting and/or the element values may required here. For other frequencies not given here, consult with a Silicon Labs representative.

If a flat Si4461 SWC TX only/split solution is required, use the TX part of the flat DT SWC match given in Table 4 on page 9.

Table 2. TX Matching Network Component Values vs. Frequency
(Split Si4461 High-Efficiency SWC TX/RX Board, V_{DD}=3.3 V, Tested with Wire-Wound Inductors)

Freq Band	Lchoke	C0	LM1	CM1	LM2	CM2	LM3
Pout = +13 dBm							
868 MHz	120 nH	47 pF	18 nH	5.1 pF	13.0 nH	3.9 pF	0 Ω
915 MHz	100 nH	39 pF	16 nH	5.1 pF	12.0 nH	3.9 pF	0 Ω
Pout = +14 dBm							
868 MHz	120 nH	47 pF	16 nH	5.1 pF	13.0 nH	3.9 pF	0 Ω
915 MHz	100 nH	39 pF	15 nH	5.1 pF	12.0 nH	3.9 pF	0 Ω
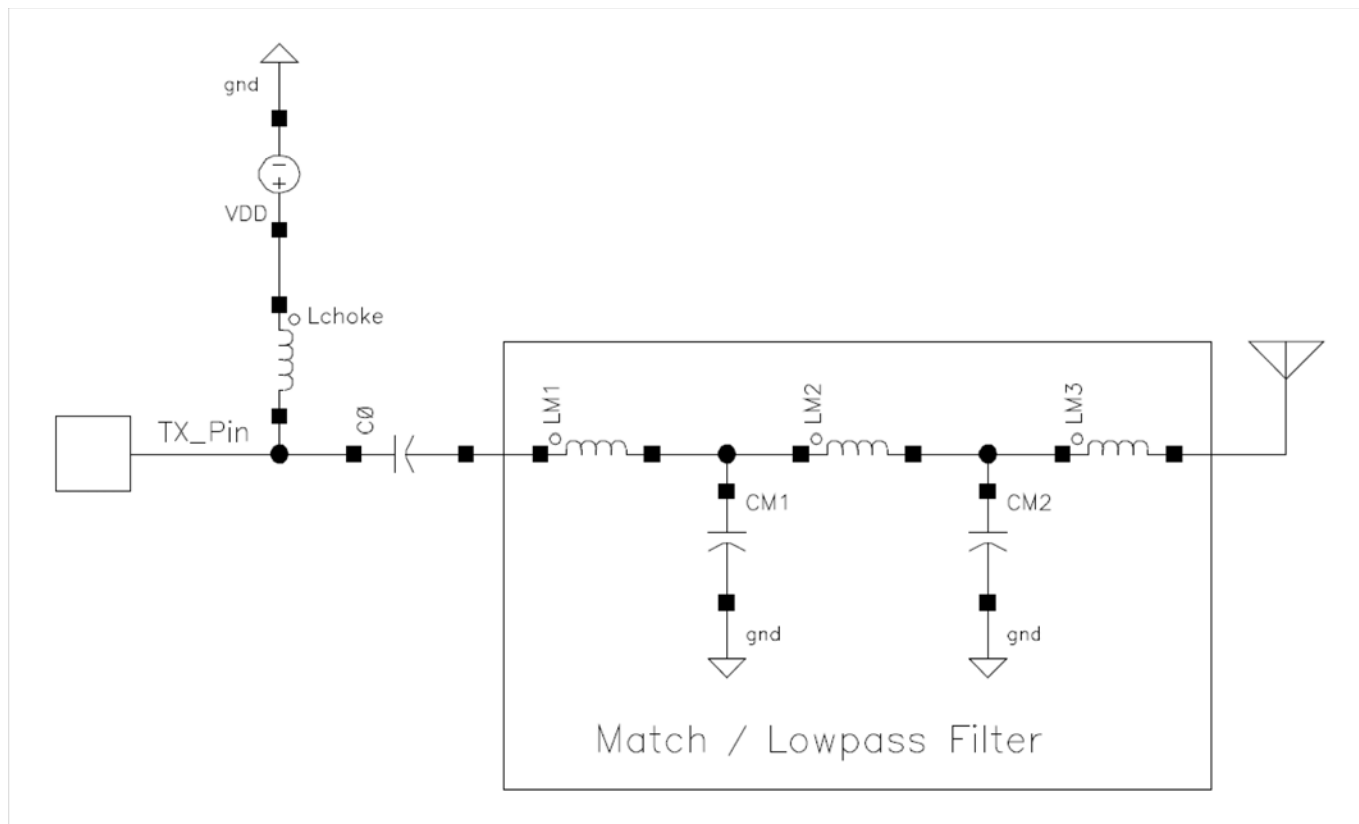
Figure 1. TX Matching Topology for Split SWC TX/RX Board Configuration

Table 3 lists summary of typical measured output power and current consumption for split board configurations given in Figure 1 and in Table 3. These results are obtained with a supply voltage of VDD = 3.3 V and with wire-wound inductors.

Table 3. Output Power and Current Consumption vs. Frequency
(Split Si4461 High-Efficiency SWC TX/RX Board, V_{DD} = 3.3 V, Tested with Wire-Wound Inductors)

Freq Band	OB[5:0]	DDAC[6:0]	Pout (dBm)	IDC (mA)
Pout = +13 dBm				
868 MHz	0x21	0x64	12.96 dBm	30.56 mA
915 MHz	0x22	0x64	12.85 dBm	30.15 mA
Pout = +14 dBm				
868 MHz	0x2C	0x64	14.10 dBm	35.61 mA
915 MHz	0x2E	0x64	14.01 dBm	36.10 mA

2.1.2. Si4461 with Direct Tie TX/RX SWC Board Configuration: Component Values and Performance

Table 4 provides the component values required for output power levels of both +13 and +14 dBm using the Single Antenna with Direct Tie SWC board configuration of Figure 2 and a supply voltage of V_{DD} = 3.3 V. One part of these matches is optimized for the best efficiency (denoted by HE in Table 4) and thus has 2–3 dB power variation in the 1.8–3.8 V Vdd range. It is still significantly better than the flatness of any CLE match.

At 868M there is also a second, flat Vdd characteristic SWC DT proposal (denoted by FC). This has 1.5 dB power variation in the 1.8–3.8 V Vdd range (see Table 7). At the time of this writing, these 4461 SWC DT matches were not tested with multilayer inductor yet. Consult with a Silicon Labs representative for other frequency SWC matches.

Table 4. Matching Network Component Values vs. Frequency
(Direct Tie Si4461 SWC Board, V_{DD} = 3.3 V, Tested with Wire-Wound Inductors)

Pout = +13 dBm											
Freq Band	**RX Side**				**TX Side**						
	LR1	**LR2**	**CR1**	**CR2**	**Lchoke**	**C0**	**LM1**	**CM1**	**LM2**	**CM2**	**LM3**	**CM3**
HE868M	20 nH	24 nH	3.0 pF	1.0 pF	120 nH	47 pF	18 nH	5.1 pF	13 nH	3.9 pF	0 Ω	N.F
HE915M	18 nH	22 nH	3.0 pF	1.0 pF	100 nH	39 pF	16 nH	5.1 pF	12 nH	3.9 pF	0 Ω	N.F.
FC868M	16 nH	16 nH	3.6 pF	1.5 pF	120 nH	47 pF	8 nH	8.2 pF	8 nH	8.2 pF	7.5 nH	3.9 pF
Pout = +14 dBm											
Freq Band	**RX Side**				**TX Side**						
	LR1	**LR2**	**CR1**	**CR2**	**Lchoke**	**C0**	**LM1**	**CM1**	**LM2**	**CM2**	**LM3**	**CM3**
HE868M	20 nH	24 nH	3.0 pF	1.0 pF	120 nH	47 pF	16 nH	5.1 pF	13 nH	3.9 pF	0 Ω	N.F.
HE915M	18 nH	22 nH	3.0 pF	1.0 pF	100 nH	39 pF	15 nH	5.1 pF	12 nH	3.9 pF	0 Ω	N.F.

A summary of typical measured output power, current consumption, and sensitivity (40 kbps, dev = 50 kHz (H = 1), 0.1% BER) for high efficiency (denoted by HE) and a 868M flat (FC) SWC direct tie board configurations of Table 4 are shown in Table 5. These results are obtained with a supply voltage of V_{DD} = 3.3 V.

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Table 5. Output Power, Current Consumption and Sensitivity vs. Frequency
(Direct Tie Si4461 SWC Board, V$_{DD}$ = 3.3 V, Tested with Wire-Wound Inductors)

Pout = +13 dBm					
Freq Band	OB[5:0]	DDAC[6:0]	Pout (dBm)	IDC (mA)	Sens. (dBm)
HE868M	0x20	0x64	12.77 dBm	30.62 mA	−109.0 dBm
HE915M	0x20	0x64	12.79 dBm	30.23 mA	−108.8 dBm
FC868M	0x27	0x7F	13.00 dBm	38.00 mA	−108.3 dBm
Pout = +14 dBm					
HE868M	0x2D	0x64	13.86 dBm	35.97 mA	−109.0 dBm
HE915M	0x2C	0x64	13.99 dBm	35.60 mA	−108.8 dBm

At all frequencies, the RX sensitivities achieved with the Direct Tie board configuration are within 1.5 dB of those obtained with the Split TX/RX board configuration. The power vs. Vdd characteristic is given for the 868M flat (FC868M) DT design in Table 6.

Table 6. Output Power, Current Consumption vs. Vdd
(Direct Tie Si4461 flat SWC Board, Wire Wound Inductors)

Vdd [V]	FC868M PA_BIAS = 0x27, PA_PWR_LVL = 0x7F	
	Pout [dBm]	Idc [mA]
1.8	11.7	34
2.1	12.5	35.6
2.4	12.8	37
2.7	12.9	37.5
3	13.1	38
3.3	13	38
3.6	13	38
3.8	13	38
delta (2.1–3.3 V)	0.5	2.4
delta (1.8–3.8 V)	1.4	4

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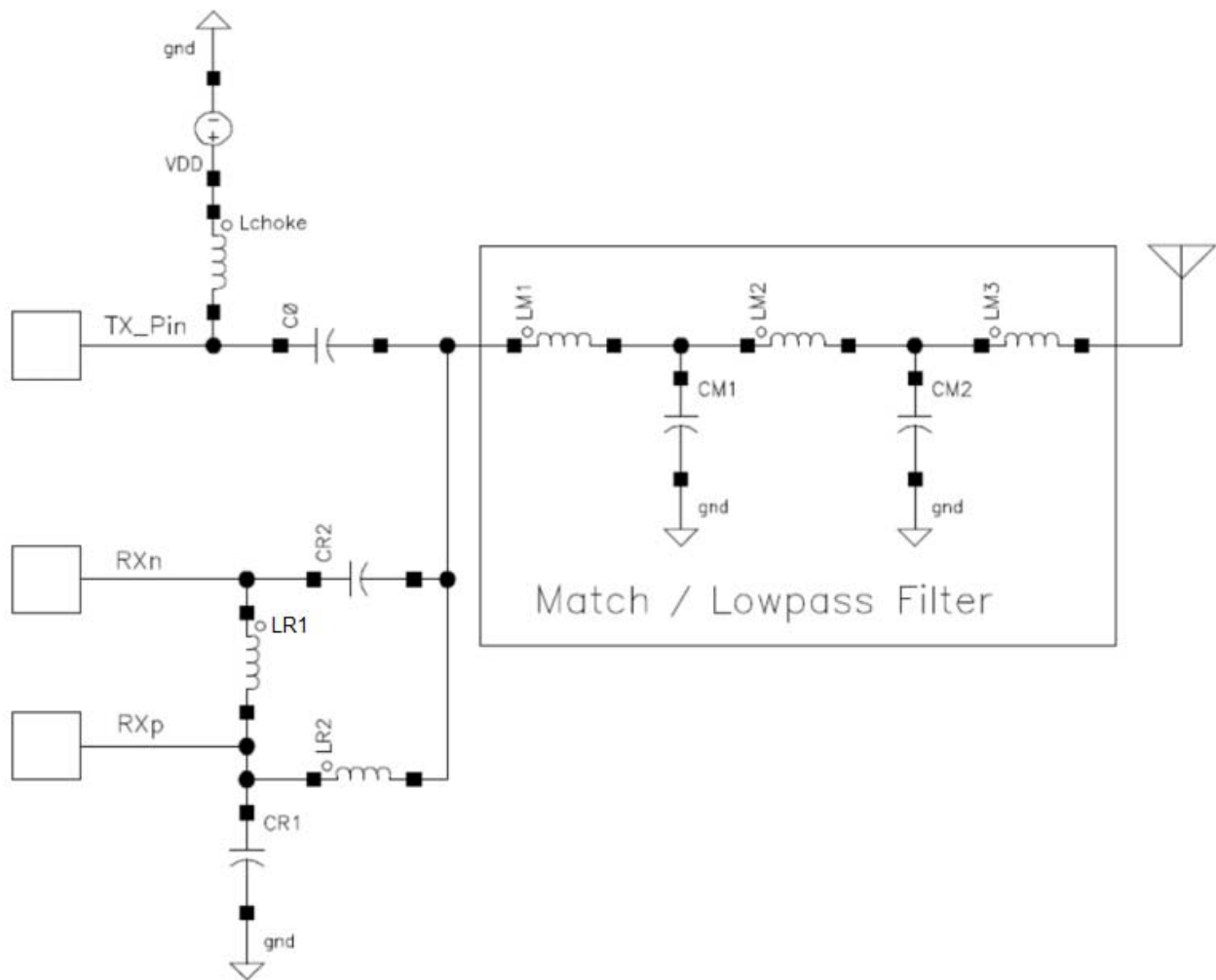
Figure 2. Matching Topology for Single Antenna with Direct Tie SWC Board Configuration

2.1.3. Si4461 CLE Split TX/RX Board Configuration: Component Values and Performance

Table 7 lists the component values required for output power levels for +14 and +16 dBm using the Split CLE TX/RX board configuration of Figure 3 and a supply voltage of V_{DD} = 3.3 V. Table 7 matching is proper for both wire-wound and multilayer type inductors. For other frequencies, consult with a Silicon Labs representative.

Table 7. TX Matching Network Component Values vs. Frequency
(Split Si4461 CLE TX/RX Board, V_{DD} = 3.3 V, Wire-Wound and Multilayer Inductor Versions)

Freq Band	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	LM3	R_{DC}
Pout = +14 dBm										
434 MHz	220 nH	15 pF	39 nH	8.2 pF	18 nH	15 pF	18 nH	6.8 pF	0 Ω	0 Ω
868 MHz	120 nH	22.0 pF	12.0 nH	4.7 pF	8.2 nH	3.9 pF	0 Ω	N.F.	0 Ω	0 Ω
Pout = +16 dBm										
434 MHz	220 nH	8.2 pF	39 nH	8.2 pF	18 nH	15 pF	18 nH	6.8 pF	0 Ω	0 Ω
868 MHz	120 nH	22.0 pF	10.0 nH	4.7 pF	8.2 nH	3.9 pF	0 Ω	N.F.	0 Ω	0 Ω

Figure 3. TX Matching Topology for Si4461 Split TX/RX Board CLE Configuration

A summary of typical measured output power and current consumption for split board configurations (both with wire-wound and multilayer inductors) is given in Table 8. These results are obtained with a supply voltage of V_{DD} = 3.3 V.
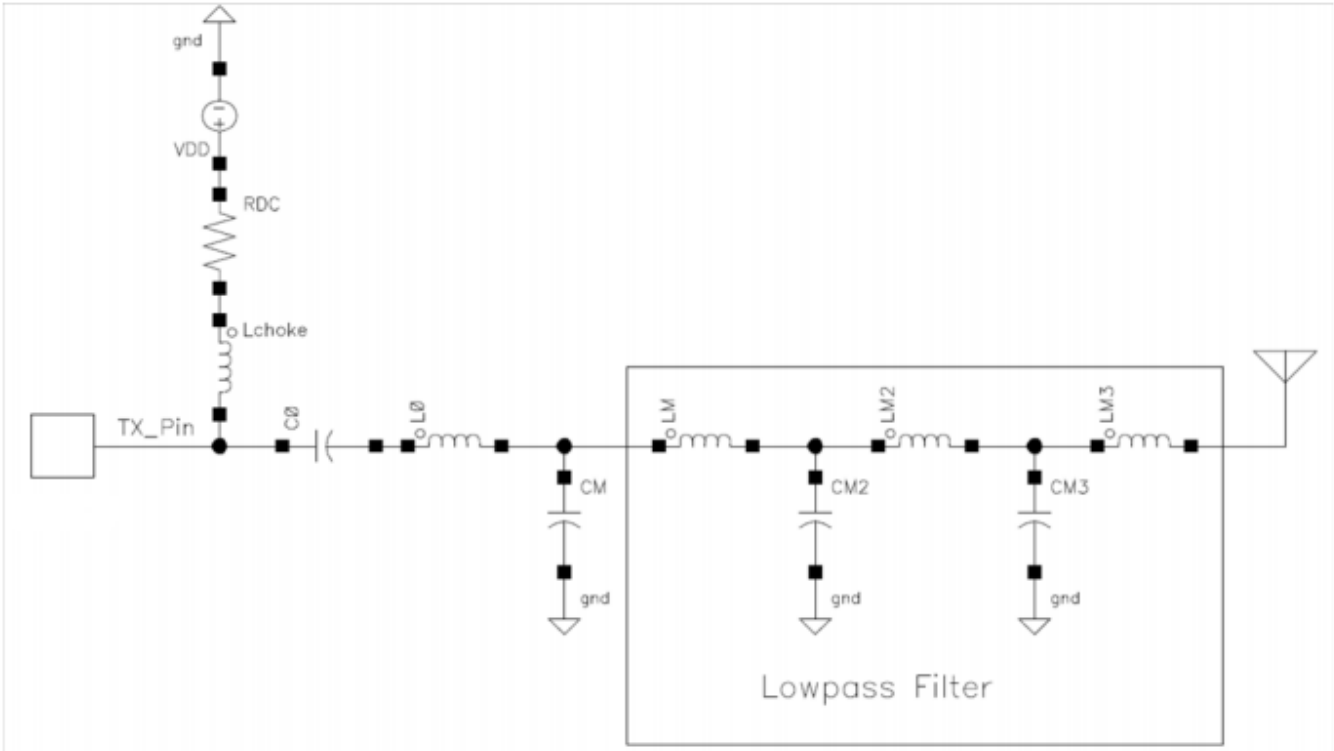
In the case of WW inductors, a lower power state setting is enough for the same output power due to the lower loss. Due to the lower power setting, the WW solution is more robust against supply voltage variations with adaptive power control. In addition, it is more robust against-load impedance variations. The efficiency is also better compared to the Multilayer matches. Moreover, with some slight component value adjustments (basically, of C0 and CM), the WW solutions can be tuned for slightly better efficiency (~2…5%) with a simultaneous sacrifice of robustness.

Table 8. Output Power and Current Consumption vs. Frequency
(Split Si4461 CLE TX/RX Board, V_{DD} = 3.3 V, Wire-Wound (WW) and Multilayer (ML) Inductor)

Freq Band	DDAC[6:0] WW	Pout WW (dBm)	IDC WW (mA)	DDAC[6:0] ML	Pout ML (dBm)	IDC ML (mA)
Pout = +14 dBm						
434 MHz	20h	14.3 dBm	28.1 mA	2Dh	14.3 dBm	29.7 mA
868 MHz	2Bh	14.4 dBm	31.6 mA	34h	14.3 dBm	34.4 mA
Pout = +16 dBm						
434 MHz	32h	16.3 dBm	35.8 mA	7Fh	16.3 dBm	38.9 mA
868 MHz	40h	16.3 dBm	38.9 mA	4Fh	16.2 dBm	42.7 mA

2.1.4. Si4461/EZR32 R61 CLE for Direct Tie Board Configuration: Component Values and Performance

Table 9 (wire-wound inductor) and Table 11 (multilayer inductor) provide the component values required for output power levels of both +14 and +16 dBm using the Single Antenna with Direct Tie board configuration of Figure 4 and a supply voltage of V_{DD} = 3.3 V. For other frequencies, consult with a Silicon Labs representative.

Table 9. Matching Network Component Values vs. Frequency
(Direct Tie Si4461 CLE Board, V_{DD} = 3.3 V, Wire-Wound Inductor)

Pout = +14 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
434 MHz	56 nH	51 nH	3.9 pF	2.2 pF	220 nH	15 pF	39 nH	8.2 pF	18 nH	15 pF	18 nH	6.8 pF	0 Ω
868 MHz	20 nH	24 nH	3.0 pF	1.0 pF	120 nH	22 pF	8.2 nH	5.6 pF	6.8 nH	5.6 pF	0 Ω	N.F.	0 Ω
Pout = +16 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
434 MHz	56 nH	51 nH	3.9 pF	2.2 pF	220 nH	15.0 pF	39 nH	8.2 pF	18 nH	15 pF	18 nH	6.8 pF	0 Ω
868 MHz	20 nH	24 nH	3.0 pF	1.0 pF	120 nH	22 pF	8.2 nH	5.6 pF	6.8 nH	5.6 pF	0 Ω	N.F.	0 Ω

Table 10. Matching Network Component Values vs. Frequency
(Direct Tie EZR32 R61 CLE Board, V_{DD} = 3.3 V, Wire-Wound Inductor)

Pout = +16 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
868 MHz	20 nH	24 nH	3.0 pF	1.0 pF	120 nH	27 pF	8.2 nH	3.9 pF	6.2 nH	10 pF	6.2 nH	5.1 pF	0 Ω

Table 11. Matching Network Component Values vs. Frequency
(Direct Tie Si4461 CLE Board, V_{DD} = 3.3 V, Multilayer Inductor)

Pout = +14 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
434 MHz	56 nH	56 nH	5.1 pF	2.7 pF	220 nH	15 pF	39 nH	8.2 pF	18 nH	15 pF	18 nH	6.8 pF	0 Ω
868 MHz	18 nH	22 nH	3.0 pF	1.2 pF	120 nH	22 pF	8.2 nH	5.6 pF	6.8 nH	5.6 pF	0 Ω	N.F.	0 Ω
Pout = +16 dBm													
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
434 MHz	56 nH	56 nH	5.1 pF	2.7 pF	220 nH	8.2 pF	39 nH	8.2 pF	18 nH	15 pF	18 nH	6.8 pF	0 Ω
868 MHz	18 nH	22 nH	3.0 pF	1.2 pF	120 nH	22 pF	8.2 nH	5.6 pF	6.8 nH	5.6 pF	0 Ω	N.F.	0 Ω
915 MHz	18 nH	22 nH	3.0 pF	1.0 pF	100 nH	22 pF	6.8 nH	3.9 pF	6.8 nH	3.9 pF	0 Ω	N.F.	0 Ω

A summary of typical measured output power, current consumption, and sensitivity in RX mode (100 kbps, H = 1, 0.1% BER) for direct tie board configurations and circuit realizations is shown in Table 12. These results are

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obtained with a supply voltage of V_{DD} = 3.3 V. The multilayer inductor version has worse efficiency.

Table 12. Output Power, Current Consumption and RX Sensitivity vs. Frequency
(Direct Tie Si4461 CLE Board, V_{DD} = 3.3 V, Wire-Wound (WW) and Multilayer (ML) Inductors)

Freq Band	DDAC[6:0] WW	Pout WW (dBm)	IDC WW (mA)	Sens WW (dBm)	DDAC[6:0] ML	Pout ML (dBm)	IDC ML (mA)	Sens ML (dBm)
				Pout = +14 dBm				
434 MHz	21h	14.4 dBm	28.7 mA	−104.7 dBm	2Fh	14.3 dBm	30.1 mA	−103.7 dBm
868 MHz	2Eh	14.3 dBm	33.2 mA	−103.5 dBm	34h	14.3 dBm	34.4 mA	−101.3 dBm
				Pout = +16 dBm				
434 MHz	3Fh	16.3 dBm	33.0 mA	−104.7 dBm	7Fh	16.4 dBm	40.1 mA	−104.0 dBm
868 MHz	41h	16.3 dBm	39.6 mA	−103.5 dBm	5Eh	16.3 dBm	42.9 mA	−101.3 dBm
915 MHz					4Fh	16.3 dBm	43.3 mA	−102.5 dBm

Table 13. Output Power, Current Consumption and RX Sensitivity vs. Frequency
(Direct Tie EZR32 R61 CLE Board, V_{DD} = 3.3 V, Wire-Wound (WW) and Multilayer (ML) Inductors)

Freq Band	DDAC[6:0] WW	Pout WW (dBm)	IDC WW (mA)	Sens WW (dBm)	DDAC[6:0] ML	Pout ML (dBm)	IDC ML (mA)	Sens ML (dBm)
				Pout = +16 dBm				
868 MHz	49h	16.1 dBm	41.4 mA	−104.5 dBm				

At all frequencies, the RX sensitivities achieved with the Direct Tie board configuration are within 2 dB of those obtained with the Split TX/RX board configuration.
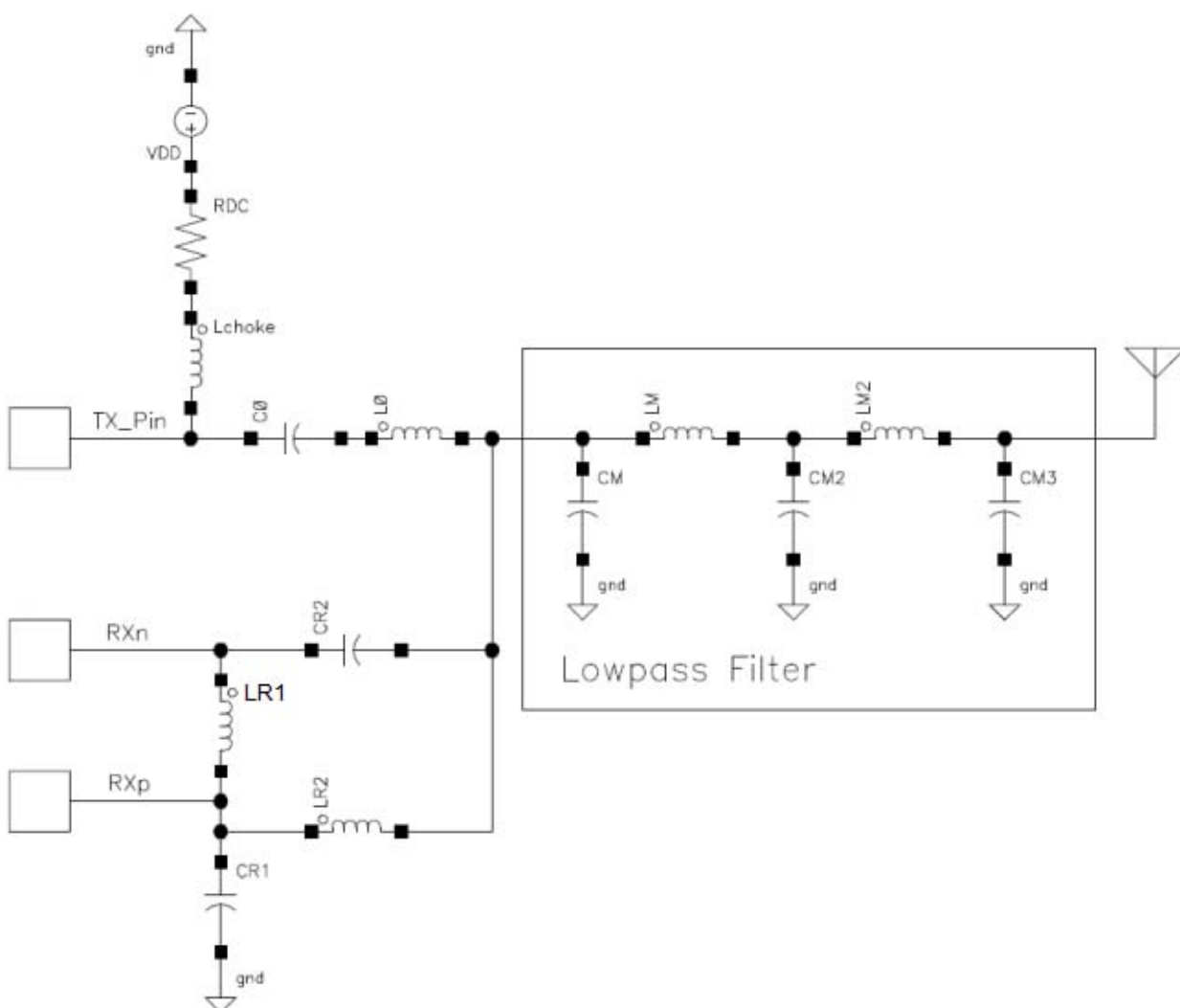
Figure 4. Matching Topology for Single Antenna with Si4461 Direct Tie CLE Board Configuration

2.2. Component Values for Si4060/Si4460/67 and EZR32 R60/67/55 Matchings

The Si4060/Si4460/67 CLE, SQW, and SWC types are typically proper for 10 dBm applications, where they have either good efficiency (CLE match with 17–19 mA total current) or stable operation (a SWC match designed for flat power characteristic has a power variation ~1 dB in the 1.8–3.8 V Vdd range). For flat Vdd characteristic (1–2 dB power variation), the CLE needs adaptive power control.

The 13 to 14 dBm regime can only be achieved with CLE matching. It has high variation over Vdd, even with adaptive power control, because it is no longer efficient due to the power setting here, which is close to the maximum. Also, with this high power, the CLE matching is sensitive to the termination impedance variations. The only advantage of these high-power Si4460/67 CLE matchings is the good efficiency.

It must be noted that all Si4060/Si4460/67 CLE matches are working in 25% duty cycle mode to achieve the best efficiency (PA_BIAS_CLKDUTY register is set to 0xC0).

The 13 dBm power CLE Si4060/4460/67 matches could work better with a 50% duty cycle, with a lower power state, i.e., with more margin. But, in this case, the current consumption would be also higher, and it would be close to that of the 13–14 dBm Si4461 CLE matches; so, with 50% duty cycle the 13 dBm Si4060/Si4460 solutions have no efficiency advantage compared to the Si4461 solutions.

2.2.1. Si4060/Si4460/67 CLE Split TX/RX Board Configuration: Component Values and Performance

Table 14 provides the component values required for output power levels for +10 and +13 dBm using the Split CLE TX/RX board configuration of Figure 5 and a supply voltage of V_{DD} = 3.3 V. The matchings of Table 14 are proper for wire-wound type inductors. For other frequencies, consult with a Silicon Labs representative. Split TX Matches using multilayer type inductors are not developed yet. For that, use the TX part of the DT matches with multilayer inductors (see Table 18). If the last inductor is only 0 Ω, a proper bypass cap can be used instead (220 pF at 434M and 56 pF at 868M) if dc blocking required. The L0 and C0 can be replaced with negligible effect.

**Table 14. TX Matching Network Component Values vs. Frequency
(Split Si4060/Si4460/67 CLE TX/RX Board, V_{DD} = 3.3 V, Wire-Wound Inductor Versions)**

| Pout = +10 dBm										
Freq Band	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	LM3	R_{DC}
434 MHz	220 nH	18 pF	56 nH	8.2 pF	18.0 nH	15.0 pF	18.0 nH	8.2 pF	0 Ω	0 Ω
868 MHz	120 nH	33 pF	8.2 nH	5.1 pF	6.8 nH	10 pF	6.8 nH	5.1pF	0 Ω	0 Ω
Pout = +13–14 dBm										
Freq Band	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	LM3	R_{DC}
434 MHz	220 nH	10 pF	56 nH	10.0 pF	18.0 nH	15.0 pF	18.0 nH	8.2 pF	0 Ω	0 Ω
868 MHz	120 nH	3.6 pF	19 nH	2.7 pF	9.1 nH	5.1 pF	9.1 nH	2.7 pF	0 Ω	0 Ω
863-921 MHz	120 nH	3.0 pF	18 nH	5.1 pF	6.8 nH	10 pF	6.8 nH	5.1 pF	0 Ω	0 Ω
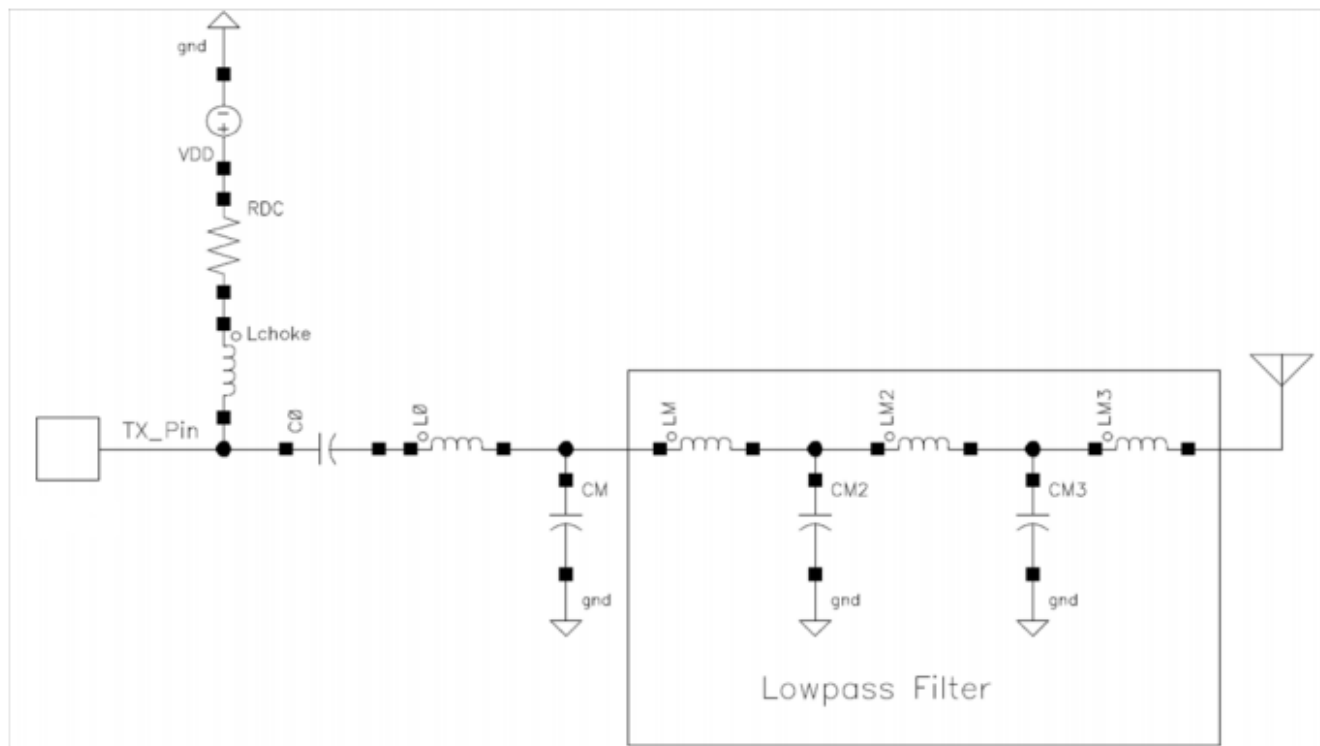
Figure 5. TX Matching Topology for Si4060/Si4460/67 Split TX/RX Board CLE Configuration

A summary of typical measured output power and current consumption for split board configurations with wire-wound inductors given in Table 15. These results are obtained with a supply voltage of V_{DD} = 3.3 V.

Table 15. Output Power and Current Consumption vs. Frequency
(Split Si4060/Si4460/67 CLE TX/RX Board, V_{DD} = 3.3 V, Wire-Wound Inductors)

Pout = +10 dBm			
Freq Band	**DDAC[6:0] WW**	**Pout WW (dBm)**	**IDC WW (mA)**
434 MHz	19h	10.4 dBm	16.9 mA
868 MHz	19h	10.3 dBm	16.4 mA
Pout = +13–14 dBm			
Freq Band	**DDAC[6:0] WW**	**Pout WW (dBm)**	**IDC WW (mA)**
434 MHz	3Fh	13.4 dBm	22.7 mA
868 MHz	3Dh	14.3 dBm	24.8 mA
863-921 at 863 MHz	36h	13.3 dBm	24.2 mA
863-921 at 921 MHz	4Ah	13.3 dBm	24.4 mA

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2.2.2. Si4460/67 and EZR32 R60/67/55 CLE for Direct Tie Board Configuration: Component Values and Performance

Table 16 provides the component values required for output power levels of both +10 and +12–13 dBm using the Single Antenna with Direct Tie board configuration of Figure 6 and a supply voltage of V_{DD} = 3.3 V. The matchings of Table 16 are proper for wire-wound type of inductors. The same is given for multilayer inductors in Table 18. For other frequencies, consult with a Silicon Labs representative. If the last inductor is only 0 Ω, a proper bypass cap can be used instead (220 pF at 434M and 56 pF at 868/915M) if dc blocking is required. The L0 and C0 can be replaced with negligible effect.

Table 16. Matching Network Component Values vs. Frequency
(Direct Tie Si4460/67 CLE Board, V_{DD} = 3.3 V, Wire-Wound Inductor)

Pout = +10 dBm												
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
434 MHz	56.0 nH	56.0 nH	5.1 pF	2.7 pF	220.0 nH	18.0 pF	56.0 nH	8.2 pF	18.0 nH	15.0 pF	18.0 nH	8.2 pF	0.0 Ω
868–915 MHz	20.0 nH	24.0 nH	3.0 pF	1.0 pF	120.0 nH	33.0 pF	8.2 nH	5.1 pF	6.8 nH	10.0 pF	6.8 nH	5.1 pF	0.0 Ω
Pout = +13 dBm												
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
434 MHz	56.0 nH	56.0 nH	5.1 pF	2.7 pF	220.0 nH	10.0 pF	56.0 nH	10.0 pF	18.0 nH	15.0 pF	18.0 nH	8.2 pF	0.0 Ω
868 MHz	20.0 nH	24.0 nH	3.0 pF	1.0 pF	120.0 nH	3.6 pF	19.0 nH	2.7 pF	9.1 nH	5.1 pF	9.1 nH	2.7 pF	0.0 Ω

Table 17. Matching Network Component Values vs. Frequency
(Direct Tie EZR32 R60/67/55 CLE Board, V_{DD} = 3.3 V, Wire-Wound Inductor)

Pout = +10 dBm												
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
434 MHz	56.0 nH	56.0 nH	5.1 pF	2.7 pF	220.0 nH	20 pF	56.0 nH	5.6 pF	18.0 nH	15.0 pF	18.0 nH	8.2 pF	0.0 Ω
Pout = +13 dBm												
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	L0	CM	LM	CM2	LM2	CM3	R_{DC}
868 MHz	20 nH	24 nH	3.0 pF	1.0 pF	120 nH	3.6 pF	19 nH	5.1 pF	6.8 nH	10 pF	6.8 nH	5.1 pF	0 Ω

**Table 18. Matching Network Component Values vs. Frequency
(Direct Tie Si4460/67 CLE Board, V_{DD} = 3.3 V, Multilayer Inductor)**

Pout = +10 dBm												
Freq Band	**RX Side**				**TX Side**								
	LR1	**LR2**	**CR1**	**CR2**	**Lchoke**	**C0**	**L0**	**CM**	**LM**	**CM2**	**LM2**	**CM3**	**RDC**
315 MHz	82 nH	68 nH	7.5 pF	3.6 pF	270 nH	12 pF	100 nH	10 pF	22 nH	18 pF	22 nH	10 pF	0.0 Ω
345 MHz	82 nH	68 nH	7.5 pF	3.6 pF	270 nH	15 pF	82 nH	10 pF	22 nH	18 pF	22 nH	10 pF	0.0 Ω
390 MHz	68 nH	68 nH	5.1 pF	2.4 pF	220 nH	18 pF	68 nH	10 pF	18 nH	18 pF	18 nH	10 pF	0.0 Ω
434 MHz	56.0 nH	56.0 nH	5.1 pF	2.7 pF	220.0 nH	18.0 pF	56.0 nH	8.2 pF	18.0 nH	15.0 pF	18.0 nH	8.2 pF	0.0 Ω
868-915 MHz	18.0 nH	22.0 nH	3.0 pF	1.2 pF	120.0 nH	33.0 pF	8.2 nH	5.1 pF	6.8 nH	10.0 pF	6.8 nH	5.1pF	0.0 Ω
Pout = +13 dBm												
Freq Band	**RX Side**				**TX Side**								
	LR1	**LR2**	**CR1**	**CR2**	**Lchoke**	**C0**	**L0**	**CM**	**LM**	**CM2**	**LM2**	**CM3**	**RDC**
434 MHz	56.0 nH	56.0 nH	5.1 pF	2.7 pF	220.0 nH	6.2 pF	56.0 nH	10.0 pF	18.0 nH	15.0 pF	18.0 nH	8.2 pF	0.0 Ω
868 MHz	18.0 nH	22.0 nH	3.0 pF	1.2 pF	120.0 nH	3.6 pF	18.0 nH	2.7 pF	9.1 nH	5.1 pF	9.1 nH	2.7 pF	0.0 Ω

The 169 MHz Class E multilayer DT match has a significantly different structure as shown in Figure 7. The element values are given in Table 19. The value of CC2 is 470 pF. Also, here, the 470 nH Lchoke inductor is a 0603 sized one because this value does not exist in the 0402 size. Currently, the 169 MHz DT match exists with multilayer inductors only.

**Table 19. Matching Network Component Values at 169 MHz
(Direct Tie Si4460/67 CLE Board, V_{DD} = 3.3 V, Multilayer Inductor)**

Pout=+10 dBm																
RX Side				**TX Side**												
LR1	**LR2**	**CR1**	**CR2**	**Lchoke**	**C0**	**L0**	**CM**	**LM**	**LM2**	**CM2**	**LM3**	**CM3**	**LM4**	**CP1**	**CP2**	**R_{DC}**
220 nH	150 nH	12.0 pF	6.2 pF	470 nH	39 pF	22 nH	6.8 pF	56 nH	47 nH	18 pF	68 nH	18 pF	47 nH	3 pF	2 pF	0 Ω

A summary of typical measured output power, current consumption and sensitivity in RX mode (100 kbps, H = 1, 0.1% BER) for direct tie board configurations and circuit realizations is shown in Table 20. These results are obtained with a supply voltage of V_{DD} = 3.3 V. The multilayer inductor versions usually has worse efficiency and sensitivity. The 13 dBm power range can be achieved at 868 and 915M with the dual band (868–915M) 10 dBm matches as well. However, for that the maximum (0x4F) power state must be used. Also, with multilayer inductors, the dual band match cannot achieve the 13 dBm at 915M.

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But, there is a possibility for tuning: by increasing the CM value (to 4.7pF), the power at maximum power state increases, and even the multilayer 10 dBm match achieves 13.1 dBm (with 26.5 mA) at 915M. However, with 4.7 pF CM, the efficiency becomes worse, and, thus, the 10 dBm power (10.2 dBm) is achieved only at power state 0x22 with 20.6 mA.

The high power (HP) 868 match can achieve the 13 dBm with large margin (i.e. in a power state significantly lower than maximum) even with multilayer inductors. Unfortunately, at 434M, even the high power match cannot achieve the 13 dBm with multilayer inductors.

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**Table 20. Output Power, Current Consumption and RX Sensitivity vs. Frequency
(Direct Tie Si4460/67 CLE Board, V$_{DD}$ = 3.3 V, Wire-Wound (WW) and Multilayer (ML) Inductors)**

Freq Band	DDAC[6:0] WW	Pout WW (dBm)	IDC WW (mA)	Sens WW (dBm)	DDAC[6:0] ML	Pout ML (dBm)	IDC ML (mA)	Sens ML (dBm)
Pout = +10 dBm								
169 MHz	TBD	TBD	TBD	TBD	23h	10.3 dBm	18.4 mA	−102.8 dBm
315 MHz	TBD	TBD	TBD	TBD	3Fh	10.3 dBm	16.9 mA	−104.5 dBm
345 MHz	TBD	TBD	TBD	TBD	34h	10.2 dBm	17.0 mA	−104.0 dBm
390 MHz	TBD	TBD	TBD	TBD	21h	10.0 dBm	16.8 mA	−104.0 dBm
434 MHz	1Ah	10.2 dBm	16.9 mA	−106.1 dBm	2Ah	10.3 dBm	17.1 mA	−103.1 dBm
868-915M, 868M op.	20h	10.5 dBm	19.7 mA	−104.2 dBm	20h	10.7 dBm	19.7 mA	−103.2 dBm
868-915M, 915M op.	20h	10.5 dBm	19.6 mA	−104.1 dBm	20h	10.3 dBm	19.3 mA	−102.9 dBm
Pout = +12…13 dBm								
434 MHz	3Fh	13.3 dBm	23.0 mA	−105.2 dBm	4Fh	12.3 dBm	23.3 mA	−104.2 dBm
868 MHz	44h	14.3 dBm	25.6 mA	−104.2 dBm	3Ch	13.3 dBm	24.1 mA	−102.0 dBm
868-915M, 868M op.	4Fh	13.7 dBm	25.5 mA	−104.2 dBm	4Fh	13.4 dBm	24.7 mA	−103.3 dBm
868-915M, 915M op.	4Fh	13.3 dBm	24.7 mA	−104.1 dBm	4Fh	12.4 dBm	23.7 mA	−103.3 dBm

**Table 21. Output Power, Current Consumption and RX Sensitivity vs. Frequency
(Direct Tie EZR32 R60/67/55 CLE Board, V$_{DD}$ = 3.3 V, Wire-Wound (WW) and Multilayer (ML)
Inductors)**

Freq Band	DDAC[6:0] WW	Pout WW (dBm)	IDC WW (mA)	Sens WW (dBm)	DDAC[6:0] ML	Pout ML (dBm)	IDC ML (mA)	Sens ML (dBm)
Pout = +10 dBm								
434 MHz	1Eh	10.1 dBm	17.7 mA	−103.9 dBm				
Pout = +13 dBm								
868 MHz	3Dh	13.2 dBm	25.0 mA	−105.2 dBm				

At all frequencies, the RX sensitivities achieved with the Direct Tie board configuration are within 2 dB of those obtained with the Split TX/RX board configuration.
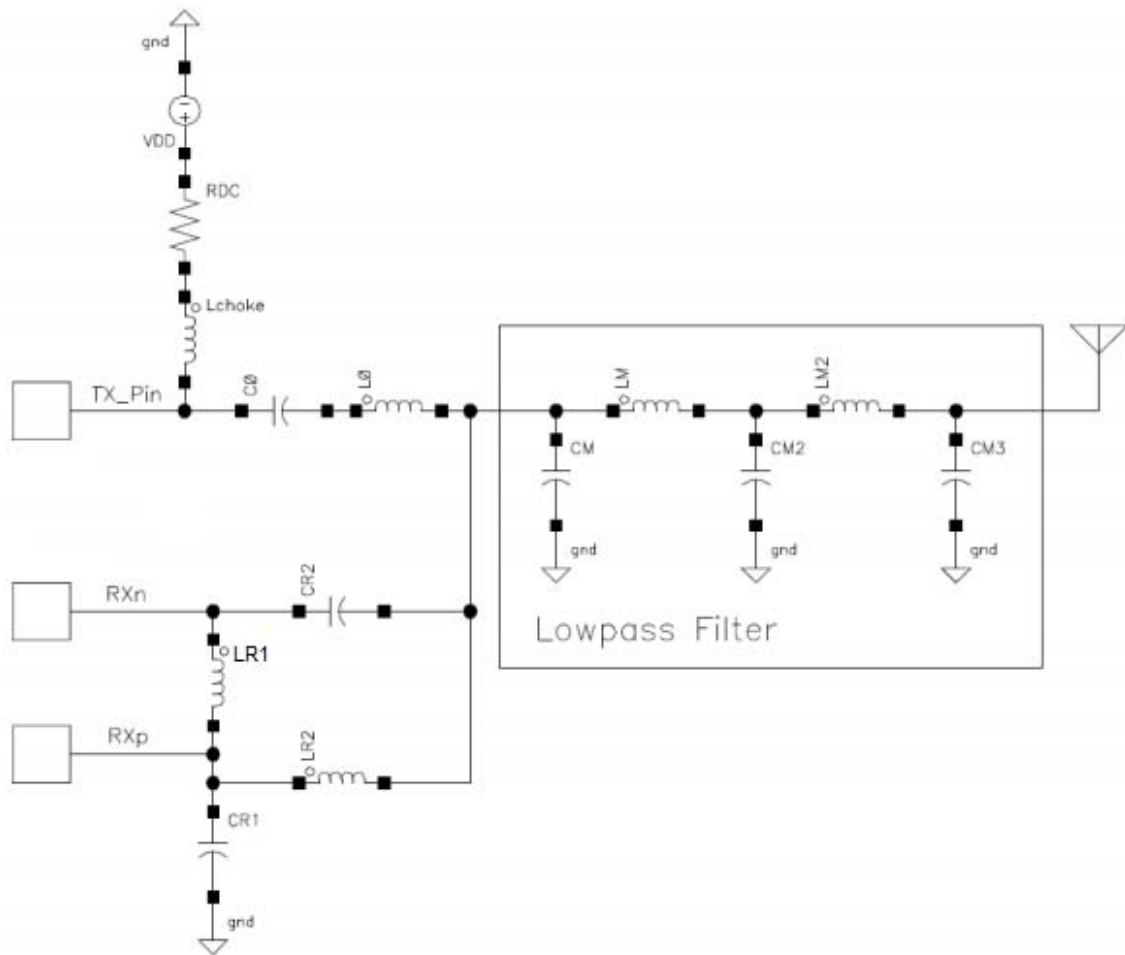
Figure 6. Matching Topology for Single Antenna with Si4460/67 Direct Tie CLE Board Configuration
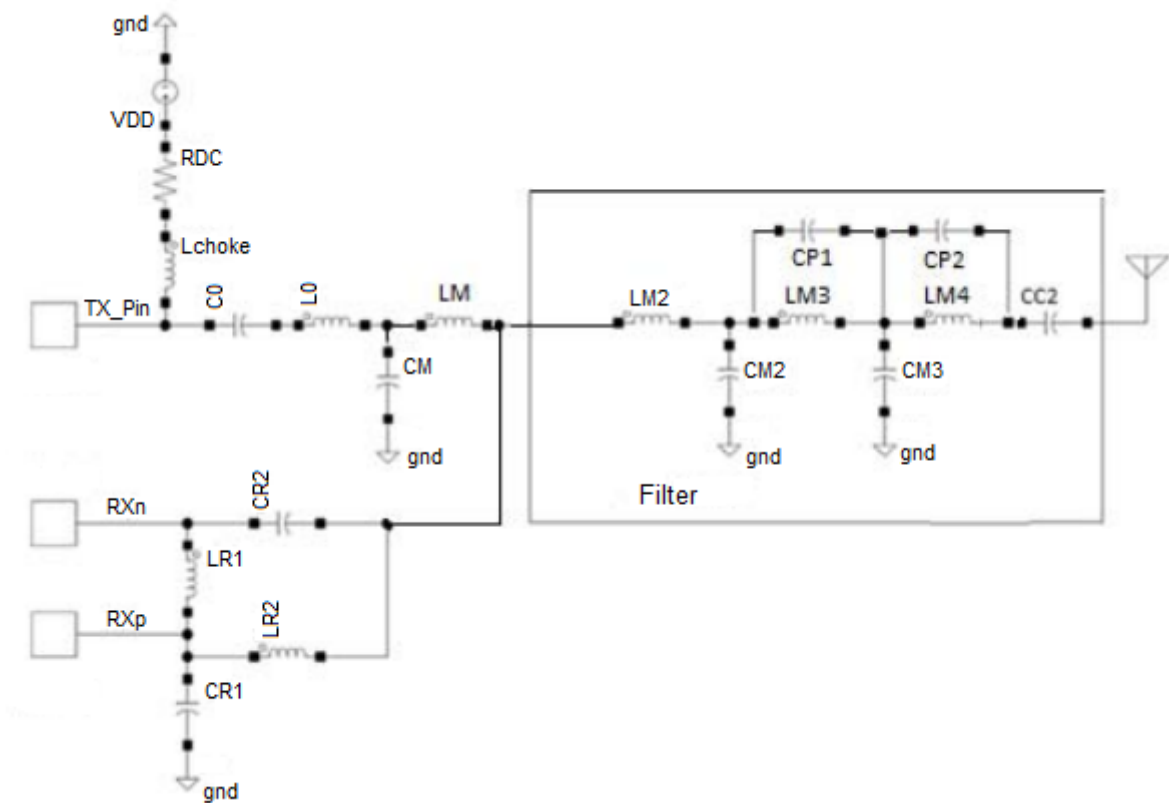
**Figure 7. Matching Topology for Single Antenna with
Si4460/67 Direct Tie CLE Board Configuration at 169 MHz**

The vdd dependency of the power of the 434M 10 dBm CLE DT is shown in Table 22. As mentioned earlier, the power of the CLE match varies with the square of the Vdd change.

**Table 22. Output Power, Current Consumption vs. Vdd
(Direct Tie Si4460/67 434M CLE Board, WW Inductors)**

Vdd	Fix Power Level 1A			Adaptive Power Level		
	power[dBm]	current[mA]	power st	power[dBm]	current[mA]	power st
3.5	10.2	17.2	1A	10.2	17.2	1A
3.3	10.2	17.1	1A	10.2	17.1	1A
3	10.1	16.6	1A	10.2	16.8	1B
2.7	9.6	16.1	1A	10.2	16.7	23
2.4	8.6	14.9	1A	9.9	16.3	4f
2.1	7.6	14.3	1A	8.8	15.5	4f
1.8	6.3	13.6	1A	7.6	14.7	4f
delta	**3.9 dB**			**2.6 dB**		
delta 2.4…3.3V	**1.6 dB**			**0.3 dB**		

Since the match works in a strongly reduced power level setting (DDAC), there is room for compensation at low Vdds. During this compensation, the power setting can be increased to reduce the internal switching loss and thus

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maintain the power as much as possible. For this, monitoring of the Vdd level is required. This so called "adaptive power control" method gives significant improvement of the Vdd flatness, especially in the most critical 2.4–3.3 V Vdd range. The result with the "adaptive power control" are also given in the table.

The flatness characteristics can be seen here to be typical for 10 dBm Si4060/4460/67 CLE and SQW matches operating on other bands as well.

At 13 dBm power levels, the Si4060/4460/67 CLE matches are working close to the maximum power state; so, the adaptive power control is not efficient there.

2.2.3. Si4060/4460/67 with Split TX\RX SWC Board Configuration: Component Values and Performance

The Si4460/67 SWC match were realized only in Direct Tie configuration. It will be detailed in section 2.2.4. If one would like to make a split TX/RX configuration or TX only match for Si4060, please use the TX path of the DT solution (Table 18). For the RX path, in split configuration, the Rx part of the CLE DT matches is recommended to use (LR1, LR2, CR1 and CR2 in Table 13 and 14) as the SWC DT matches may use other than 50 Ω RX match input impedances.

The power and current consumption of the split solution in TX mode is very close to the DT results (Table 19).

Important to note that these SWC matches are designed for flat (dP<~1.2 dB in the 1.8…3.8 V Vdd range) power and not for the highest efficiency. Due to this the impedance level of the match is lower and thus requires higher current for the same power.

2.2.4. Si4460/67 with Direct Tie TX/RX SWC Board Configuration: Component Values and Performance

Table 23 provides the component values required for output power levels of +10 dBm, using the Single Antenna with Direct Tie SWC board configuration of Figure 8 and a supply voltage of VDD = 3.3 V. The matches are working with low cost multilayer inductors. For other frequencies pls. consult with a Silicon Labs representative.

Table 23. Match Network Component Values vs. Frequency
(Direct Tie Si4460/67 SWC Board, VDD = 3.3 V, Multilayer Inductors)

Pout = +10 dBm												
Freq Band	RX Side				TX Side								
	LR1	LR2	CR1	CR2	Lchoke	C0	CM	LM	CM2	LM2	CM3	LM3	CM4
315 MHz	82 nH	68 nH	7.5 pF	3.6 pF	270 nH	470 pF	3.9 pF	27 nH	8.2 pF	22 nH	8.2 pF	0 Ω	N.F.
434 MHz	56 nH	56 nH	5.1 pF	2.7 pF	220 nH	270 pF	1.8 pF	22 nH	8.2 pF	18 nH	15.0 pF	18.0 nH	8.2 pF
868 MHz	18 nH	27 nH	3.0 pF	1.2 pF	120 nH	68 pF	N.F.	8.2 nH	5.1 pF	6.2 nH	5.1 pF	0 Ω	N.F.
915 MHz	18 nH	22 nH	3.0 pF	1.0 pF	100 nH	56 pF	N.F.	6.8 nH	3.9 pF	6.8 nH	3.9 pF	0 Ω	N.F.

The value of CC1 capacitor is equal to the value of C0 in Table 23.

A summary of typical measured output power, current consumption and sensitivity (100 kbps, H = 1, 0.1% BER) for direct tie board configurations and circuit realizations is shown in Table 24. These results are obtained with a supply voltage of VDD = 3.3 V.

Table 24. Output Power, Current Consumption and Sensitivity vs. Frequency
(Direct Tie Si4460/67 SWC Board, VDD = 3.3 V, Multilayer Inductors)

Pout = +10 dBm					
Freq Band	OB[5:0]	DDAC[6:0]	Pout (dBm)	IDC (mA)	Sens. (dBm)
315 MHz	0x21	0x44	10.28 dBm	23.50 mA	–103.9 dBm
434 MHz	0x2B	0x44	10.40 dBm	26.60 mA	–103.5 dBm

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**Table 24. Output Power, Current Consumption and Sensitivity vs. Frequency
(Direct Tie Si4460/67 SWC Board, VDD = 3.3 V, Multilayer Inductors)**

868 MHz	0x1E	0x44	10.50 dBm	23.70 mA	–102.0 dBm
915 MHz	0x22	0x44	10.40 dBm	24.20 mA	–102.7 dBm

At all frequencies, the RX sensitivities achieved with the Direct Tie board configuration are within 1.5 dB of those obtained with the Split TX/RX board configuration.

The Vdd dependency of the flat SWC 4460/67 designs are given in Table 25. The flatness is 0.5…0.8 dB and 1–1.2 dB in the 2.1…3.3 V and 1.8…3.8 V Vdd range, respectively.

**Table 25. Output Power, Current Consumption vs. Vdd
(Direct Tie Si4460/67 SWC Board, Multilayer Inductors)**

Vdd [V]	315M 4460TSC10D315, PA_BIAS = 0x21, PA_PWR_LVL = 0x44		434M 4460TSC10D434, PA_BIAS = 0x2B, PA_PWR_LVL = 0x44		868M 4460TSC10D868, PA_BIAS = 0x1E, PA_PWR_LVL = 0x44		915M 4460TSC10D915, PA_BIAS = 0x22, PA_PWR_LVL = 0x44	
	Pout [dBm]	Idc [mA]	Pout [dBm]	Idc [mA]	Pout [dBm]	Idc [mA]	Pout [dBm]	Idc [mA]
1,8	9.34	22.2	9.34	24.83	9.28	22.7	9.27	23.76
2.1	9.85	22.53	9.95	25.3	9.66	22.72	9.68	23.52
2.4	10.15	22.89	10.26	25.76	10.15	23.07	9.97	23.67
2.7	10.27	23.31	10.39	26	10.28	23.2	10.23	24.04
3	10.28	23.39	10.39	26.46	10.48	23.59	10.39	24.15
3.3	10.28	23.45	10.4	26.6	10.5	23.66	10.44	24.2
3.6	10.28	23.54	10.4	26.7	10.5	23.73	10.49	24.33
3.8	10.29	23.62	10.4	26.83	10.51	23.8	10.5	24.4
delta (2.1–3.3 V)	0.43 dB	0.92	0.45 dB	1.3	0.84 dB	0.94	0.76 dB	0.68
delta (1.8–3.8 V)	0.95 dB	1.42	1.06 dB	2	1.23 dB	1.1	1.23 dB	0.64
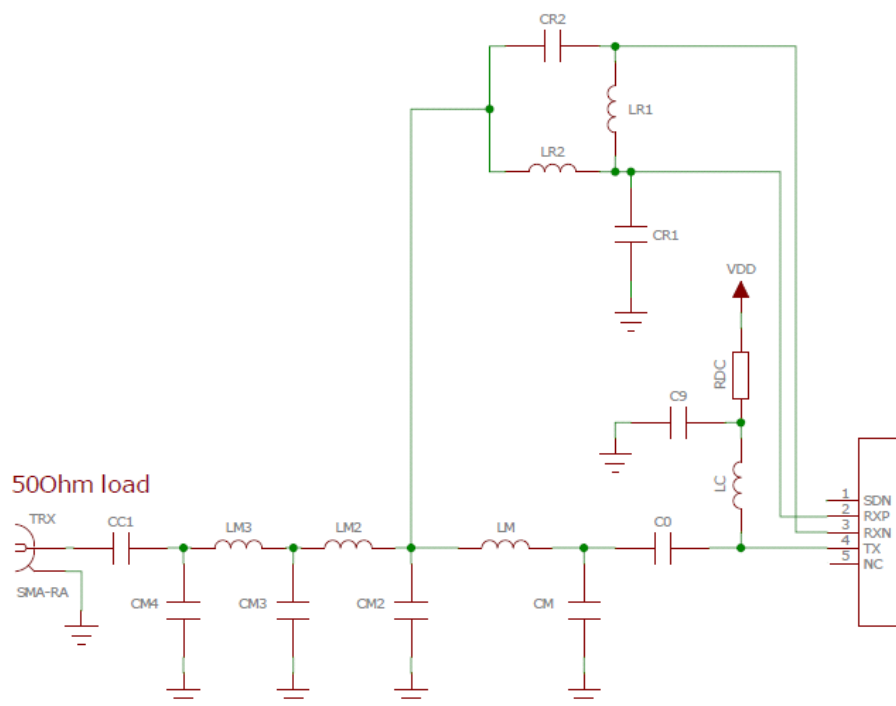
Figure 8. Matching Topology for Single Antenna with Direct Tie SWC Board Configuration

3. Switched Current (SWC) Matching Procedure Overview

3.1. SCW Matching Design for Split TX/RX Boards

In this section, the procedure for matching the Si4461 RFIC on a Split TX/RX board with SWC matching type is discussed in detail. The Si4060/Si4460/67 SWC matching use the same procedure only the target external load impedance is different due to the lower power level and lower IC shunt output capacitance. The main steps in the matching procedure are summarized below:

1. Measure the typical PA shunt output capacitance (C_{PA}) and resistance (R_{PA}) of the chip.
2. Choose L_{CHOKE} (pull-up inductor) for high impedance at the desired frequency of operation.
3. Select/calculate internal load resistance R_{LOAD_INT} for the desired output power level.
4. Calculate PA bias current setting.
5. Calculate required external load impedance Z_{LOAD} to present to the TX pin.
6. Construct a simple 2-element L-C matching network to transform the antenna load impedance (typically R_{ANT} = 50 Ω) to the calculated PA load impedance Z_{LOAD}.
7. Add sections of lowpass filtering (while maintaining the desired impedance transformation ratio), necessary to attenuate the harmonic levels below the applicable regulatory standard.

3.1.1. Measurement of PA Shunt Output Capacitance/Resistance (C_{PA}/R_{PA})

The output of the PA may be modeled as a shunt resistor R_{PA} in parallel with a shunt capacitor C_{PA} as illustrated in Figure 9. The values of R_{PA} and C_{PA} are not constant but instead vary over the frequency range of the Si4461 chip. It is necessary to determine the values of both R_{PA} and C_{PA} prior to constructing a matching network. The shunt output capacitance and resistance of the PA may be measured using a network analyzer.
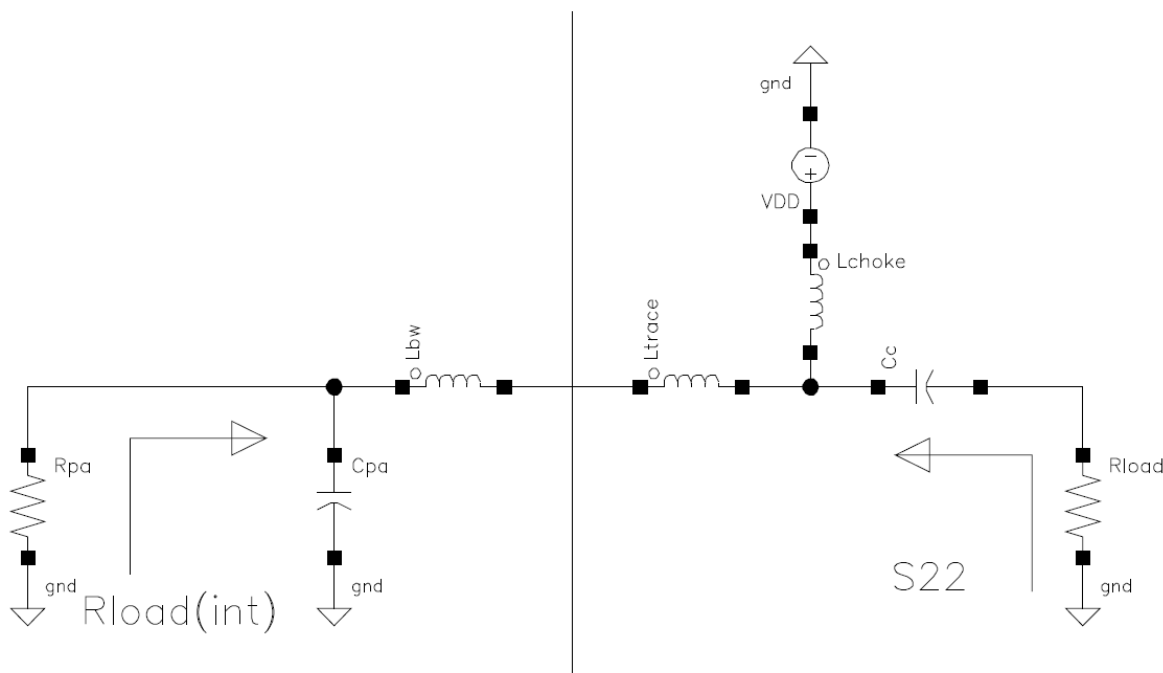
Figure 9. Model of PA Output Circuit and Impedance Measurement Network

DC bias to the PA output circuit is provided through a pull-up inductor, L_{CHOKE}. The value of this pull-up inductor should be chosen to present a very high impedance at the desired frequency of operation, such that it has no effect upon the impedance measurement. The inductance value should not be so large as to already be at (or past) parallel self-resonance at the desired operating frequency. The exact inductance value is not critical; however, Silicon Labs recommends the following range of inductance values (assuming 0402-size or 0603-size inductors) as a function of the desired operating frequency:

- 315 MHz: approximately 270 to 390 nH
- 470 MHz: approximately 220 nH
- 868 MHz: approximately 120 nH
- 915 MHz: approximately 100 nH

The network analyzer is connected to the TX output pin and pull-up inductor through a dc blocking capacitor to ensure that the VDD supply voltage does not damage the port of the network analyzer. The Si4461 chip is configured for CW TX operation at a frequency close to (but not directly at) the desired frequency of operation. The reason for this is that the chip is transmitting a signal (although at lower power) that is not correlated with the swept signal from the network analyzer. The network analyzer displays this anomalous signal as a "spike" in the S-parameter curve with the amplitude of the spike growing as the output power is increased. Thus, it is convenient to move this spike slightly to one side of the frequency at which we desire to place the measurement marker. Also, it is advisable to configure the chip for a relatively low value of output power in order to prevent damage to the input of the network analyzer. By trial-and-error, one can observe that the value of shunt output capacitance and resistance does not appear to be significantly influenced by the number of PA device fingers selected (i.e., PA_DDAC property setting).
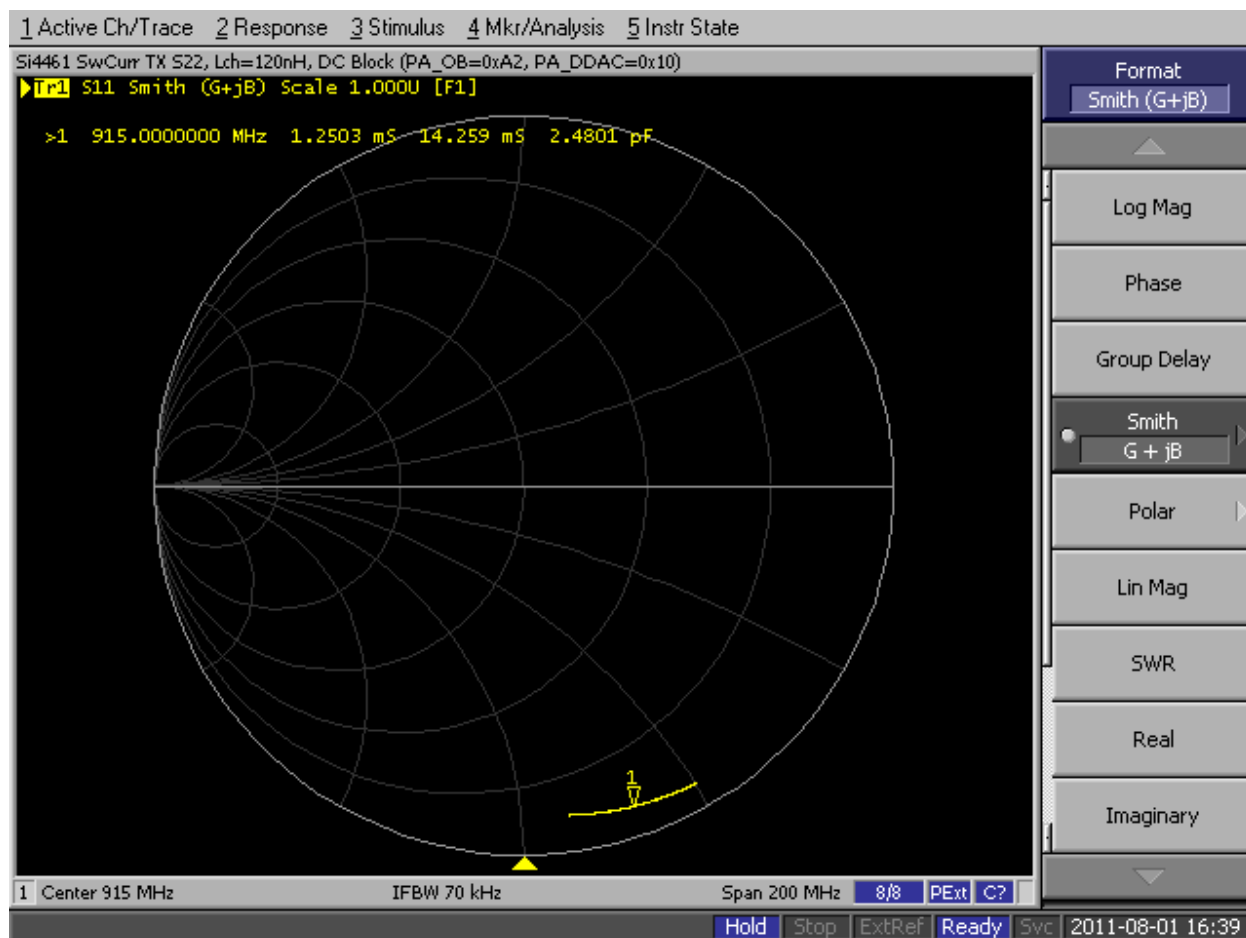
Figure 10. Si4461 PA Shunt Output Capacitance at 915M (TX Mode)

The plot of Figure 10 illustrates the measured value of output admittance (with L_{CHOKE} = 100 nH) at 915 MHz to be $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 1.25 + j14.26 ms. The output admittance may be measured at each desired frequency (with an appropriate selection of pull-up inductor L_{CHOKE}) and is found to be the following:

- 169 MHz (L_{CHOKE} = 470 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 0.010 + j1.79 ms
- 315 MHz (L_{CHOKE} = 390 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 0.207 + j2.87 ms
- 470 MHz (L_{CHOKE} = 220 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 0.291 + j4.96 ms
- 868 MHz (L_{CHOKE} = 120 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 1.07 + j12.93 ms
- 915 MHz (L_{CHOKE} = 100 nH): $Y_{OUT} = G_{OUT} + jB_{OUT}$ = 1.25 + j14.26 ms

These admittance values are quite repeatable from chip to chip; so, these published values may be used by the designer without the need to remeasure each application.

However, it is apparent that this measured value of output admittance does *not* represent the equivalent internal shunt PA capacitance and resistance. This is due to the impedance-transforming effect of the series bond wire and trace inductance as illustrated in Figure 9. As seen from outside the chip, the apparent value of shunt PA resistance will appear to be lower than the actual internal value. Additionally, the apparent value of shunt PA capacitance will appear to be higher than the actual internal value.

The actual internal values may be calculated if the total value of series inductance ($L_{SERIES} = L_{BW} + L_{TRACE}$) is known. Although this value of inductance is not known precisely, it is reasonably estimated to be L_{SERIES} = 2.9 nH (L_{BW} = 1 nH, L_{TRACE} = 1.9 nH). With a bit of mathematical manipulation, the formulas for the equivalent internal PA resistance and capacitance values may be derived as follows:

$$Z_{OUT} = R_{OUT} + jX_{OUT} = \left(\frac{1}{Y_{OUT}}\right) = \left(\frac{1}{G_{OUT} + jB_{OUT}}\right)$$

Equation 1.

$$R_{OUT} = \left(\frac{G_{OUT}}{G_{OUT}^2 + B_{OUT}^2}\right)$$

Equation 2.

$$X_{OUT} = \left(\frac{-B_{OUT}}{G_{OUT}^2 + B_{OUT}^2}\right)$$

Equation 3.

$$Z_{OUT} = R_{OUT} + jX_{OUT} = \left(\frac{1}{G_{PA} + jB_{PA}}\right) + jX_{L_{SERIES}}$$

Equation 4.

$$G_{PA} + jB_{PA} = \left(\frac{1}{R_{OUT} + jX_{OUT} - jX_{L_{SERIES}}}\right)$$

Equation 5.

$$G_{PA} = \frac{1}{R_{PA}} = \frac{R_{OUT}}{R_{OUT}^2 + (X_{OUT} - X_{L_{SERIES}})^2}$$

Equation 6.

$$B_{PA} = 2\pi f C_{PA} = \frac{X_{L_{SERIES}} - X_{OUT}}{R_{OUT}^2 + (X_{OUT} - X_{L_{SERIES}})^2}$$

Equation 7.

From these equations, the following values of internal PA shunt resistance and capacitance are obtained:

- 169 MHz: R_{PA} = 101 kΩ, C_{PA} = 1.68 pF
- 315 MHz: R_{PA} = 4991 Ω, C_{PA} = 1.427 pF
- 470 MHz: R_{PA} = 3735 Ω, C_{PA} = 1.611 pF
- 868 MHz: R_{PA} = 1356 Ω, C_{PA} = 1.970 pF
- 915 MHz: R_{PA} = 1226 Ω, C_{PA} = 2.006 pF

3.1.1.1. Impedance Values for Si4060/Si4460/67 SWC Configurations

As mentioned earlier, the SWC match design process flow is the same for the Si4060/Si4460/67, but the chip output impedance, power level, current magnitude (and thus the R_{LOAD_INT}) are different. In this step, the measured Si4060/Si4460/67 output admittances and internal RC equivalents are given:

The Si4060/Si4460/67 output admittance is measured at each desired frequency (with an appropriate selection of pull-up inductor L_{CHOKE}) and is found to be as follows:

- 169 MHz (L_{CHOKE} = 470 nH): Y_{OUT} = G_{OUT} + jB_{OUT} = 0.75 + j1.01 ms
- 315 MHz (L_{CHOKE} = 390 nH): Y_{OUT} = G_{OUT} + jB_{OUT} = 0.18 + j1.74 ms
- 434 MHz (L_{CHOKE} = 220 nH): Y_{OUT} = G_{OUT} + jB_{OUT} = 0.25 + j2.36 ms
- 470 MHz (L_{CHOKE} = 220 nH): Y_{OUT} = G_{OUT} + jB_{OUT} = 0.25 + j2.88 ms
- 868 MHz (L_{CHOKE} = 120 nH): Y_{OUT} = G_{OUT} + jB_{OUT} = 0.79 + j7.57 ms
- 915 MHz (L_{CHOKE} = 100 nH): Y_{OUT} = G_{OUT} + jB_{OUT} = 0.84 + j7.85 ms

The Si4060/Si4460 internal PA shunt resistance and capacitance values are obtained via Equations 1 to 7:

- 169 MHz: R_{PA} = 1330 Ω, C_{PA} = 0.95 pF
- 315 MHz: R_{PA} = 5670 Ω, C_{PA} = 0.87 pF
- 434 MHz: R_{PA} = 4100 Ω, C_{PA} = 0.85 pF
- 470 MHz: R_{PA} = 4150 Ω, C_{PA} = 0.95 pF
- 868 MHz: R_{PA} = 1590 Ω, C_{PA} = 1.24 pF
- 915 MHz: R_{PA} = 1530 Ω, C_{PA} = 1.21 pF

3.1.2. Selection/Calculation of R_{LOAD_INT}

Successfully obtaining the desired level of output power while minimizing current consumption or achieving Vdd flatness depends strongly upon the load resistance presented to the PA. However, it is important to distinguish between the load impedance presented to the TX pin (R_{LOAD}) and the impedance present at the drain of the output devices internal to the chip (R_{LOAD_INT}). These values are different due to the impedance-transforming effect of the series bond wire inductance and trace inductance (discussed in the previous section). It is apparent that, due to the series inductance (L_{BW}-L_{TRACE}) and internal shunt PA capacitance (C_{PA}), the effective internal load resistance R_{LOAD_INT} is larger than R_{LOAD}. The total internal load resistance (R_{TOTAL}) seen by the PA output device is the parallel combination of R_{PA} and R_{LOAD_INT}.

The power extracted from the PA output devices may be readily calculated as $P_{PA} = I_{PA}^2 \times R_{TOTAL}$. Note that the power sourced from the PA output devices (P_{PA}) is not the same as the power delivered (P_{OUT}) to the load impedance, R_{LOAD}, because some power is dissipated in the internal PA resistance, R_{PA}. For a given value of PA output current I_{PA}, the output power may be increased by presenting a larger total load impedance. Obviously, this statement only holds true for sufficiently small values of R_{TOTAL}, such that clipping of the peaks of the drain voltage waveform does not occur. That is to say, the voltage swing at the drain of the output device must be held to a reasonably low value. A reasonable design constraint is to keep the peak drain voltage swing at $V_{PK} \leq V_{DD} - 0.7$ V. This provides some voltage headroom on the output devices to ensure they remain in a linear region and continue to operate as switched current sources. It also allows for some tolerance against variations in supply voltage; if the output devices remain in a linear operating region, the output power is not significantly a function of supply voltage. The voltage peak at the internal drain node is *not* the same value as may be measured at the TX output pin of the device (again due to the impedance transforming effects of the series inductance).

It is also clear that, if the desired output power level is low enough, drain voltage clipping is not a concern. There are many combinations of I_{PA} and R_{TOTAL} that will theoretically provide the target value of P_{PA} and thus also P_{OUT}. Optimal current efficiency is obtained by selecting the lowest possible value of I_{PA} (i.e., highest value of R_{TOTAL}) that will result in a drain voltage waveform that remains just below clipping amplitude at the operation supply voltage. However, if the design target is the flat power vs. Vdd characteristic, the load impedance has to be decreased to avoid clipping even at the lowest possible supply level. In this case, the current efficiency will not be optimal at higher Vdd levels because the target power is achieved with lower voltage swing (and higher current magnitude) optimized for the low Vdd level. In other words, efficiency has to be sacrificed to achieve flatness.

On the other side, If the design target is the highest efficiency at a given supply voltage, the value of R_{TOTAL} cannot be made arbitrarily large; it is self-evident that it cannot be larger than the internal equivalent parallel resistance of the PA itself (R_{PA}). The limiting case would occur if the transformed value of load impedance (R_{LOAD_INT}) was infinite, such that $R_{TOTAL} = R_{PA} // R_{LOAD\_INT} \approx R_{PA}$. In such a case, all of the output power would be dissipated in the output devices themselves rather than being delivered to the load impedance. Thus, the incremental benefit to PA efficiency diminishes as R_{LOAD} (and thus R_{LOAD_INT}) is raised to higher and higher values.

The output impedance measurements of the previous section indicate that the internal parallel output resistance of the PA output device is $R_{PA} = 1226 \ \Omega$ (using the Si4461 at 915 MHz as an example. For the Si4060/4460/67, the Rpa is 1530 Ω). It is desirable to present an effective internal load impedance, R_{LOAD_INT}, that is significantly lower than the PA output resistance itself so that most of the power is delivered to the load and not dissipated in the PA output devices. However, this constraint is weakly defined; so, there are many possible values of R_{LOAD_INT} that could be considered as satisfactory. It is necessary to provide further design constraints or "rules of thumb" in order to select an appropriate value of R_{LOAD_INT}.

One factor to consider is the impedance transformation factor required from the external matching network. The antenna load impedance (into which the output power must eventually be delivered) is typically a low value, such as 50 Ω. The external matching network must transform this antenna impedance (R_{ANT}) into the load impedance (R_{LOAD}) seen at the TX pin, which is then further transformed by the series bond wire/trace inductance into the internal load resistance (R_{LOAD_INT}). The Q-factor of the external matching network is approximately proportional to the square root of the ratio R_{LOAD}:R_{ANT}, and thus, as R_{LOAD} is made larger, the required Q-factor of the external network also increases. If the required impedance transformation ratio is too large, the loss of the external matching network may increase, and tuning of the circuit may become sensitive to component tolerances.

An additional factor to consider is the amount of power dissipated in the internal PA devices that is considered acceptable. This is a loss term that decreases current efficiency; so, it is desirable to make it as small as possible.

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As the internal PA resistance R_{PA} is not infinite, this loss term cannot be made zero. However, it can be minimized by making the value of R_{LOAD_INT} small in comparison to R_{PA}, such that most of the power is delivered to the output load and not dissipated in the PA devices.

Thus the selection criteria for R_{LOAD_INT} may be summarized as follows:

- A large value of R_{LOAD_INT} increases R_{TOTAL}, thereby improving the current efficiency (by requiring a lower value of I_{PA} for a given target value of P_{PA}).

- A small value of R_{LOAD_INT} decreases the percentage of power dissipated in the internal PA resistance.

- A small value of R_{LOAD_INT} decreases the impedance transformation ratio required from the external matching network, thus decreasing losses due to finite Q of discrete components and improving sensitivity to component tolerances.

- A small value of R_{LOAD_INT} ensures that the peak drain voltage does not exceed levels where clipping may occur. This is the most important condition for flat power vs. Vdd characteristic, even at the lowest Vdd limit.

Given these somewhat conflicting design goals, the selection of R_{LOAD_INT} is made as a compromise to partially satisfy all four criteria and is stated as the following rule-of-thumb:

R_{LOAD_INT} shall be chosen as large as possible while not exceeding $R_{PA}/5$ or 5 x R_{ANT}, while remaining low enough to ensure $V_{PK} < V_{DD} - 0.7$ V (with flat VDD design, the VPK can be fine-tuned during bench evaluation to satisfy the specification).

In the Si4461 high-efficiency match design example at 915 MHz with R_{PA} = 1226 Ω, R_{ANT} = 50 Ω, and a target output power level of +14 dBm, this rule of thumb leads to choosing $R_{LOAD\_INT} \approx 90$ Ω (limited by the V_{PK} design constraint at 3.3 V Vdd, as will be shown shortly). A larger value of R_{LOAD_INT} may be selected if the target output power level is reduced (e.g., $R_{LOAD\_INT} \approx 120$ Ω for P_{OUT} = +13 dBm). Similarly, for +10 dBm high-efficiency Si4060/Si4460/67 SWC solutions, $R_{LOAD\_INT} \approx 240$ Ω is the optimum. For flat power design, the optimum impedance is around 50 Ω for 13 dBm and 120–140 Ω for 10 dBm.

3.1.3. Calculation of PA Bias Current I_{PA}

The total load resistance is readily calculated as the parallel combination of R_{LOAD_INT} and R_{PA}. In our Si4461 14 dBm example:

$$R_{TOTAL} = \frac{1}{\left(\frac{1}{R_{PA}}\right) + \left(\frac{1}{R_{LOAD\_INT}}\right)} = \frac{1}{\left(\frac{1}{1226}\right) + \left(\frac{1}{90}\right)} = 83.84 \ \Omega$$

Equation 8.

The finite value of R_{PA} implies that some output power will be internally dissipated in the output device itself, and thus the power delivered to the load will be less than that obtained from straightforward calculations of $P = I^2$ x R. This loss factor may be calculated as:

$$P_{LOSS\_INT} = 10 \log\left(\frac{R_{PA}}{R_{PA} + R_{LOAD\_INT}}\right) = 10 \log\left(\frac{1226}{1226 + 90}\right) = -0.31 \ dB$$

Equation 9.

This internal loss is unavoidable; it is simply necessary to adjust the PA bias current for a higher level in order to compensate for this power loss.

If the external matching network is assumed to be lossless (i.e., discrete matching components with infinite Q), the only loss in the circuit is due to P_{LOSS_INT}. For a target output power P_{OUT} delivered to the load, the PA current may be calculated as the following:

$$I_{PA} = \sqrt{\frac{P_{PA}}{R_{TOTAL}}} = \sqrt{\frac{P_{OUT} - P_{LOSS}}{R_{TOTAL}}}$$

Equation 10.

If the desired output power level is chosen as P_{OUT} = +14 dBm = 25 mW, P_{PA} = 14.0 + 0.31 = 14.31 dBm = 27.0 mW and the PA current may be calculated as follows:

$$I_{PA} = \sqrt{\frac{0.0270}{83.84}} = 17.95 \text{ mA}$$

Equation 11.

Thus, I_{PA} = 17.95 mA (RMS) or 25.38 mA peak current (50.76 mA pk-pk) at the fundamental frequency. This current amplitude would theoretically result in peak *internal* drain voltage swing of V_{PEAK} = I_{PA_PEAK} x R_{TOTAL} = 25.38 mA x 83.84 Ω = 2.13 Vpk. This peak drain voltage swing appears acceptably small to ensure linearity (non-clipping), assuming a supply voltage of VDD ≥ V_{PEAK} + 0.7 V = 2.83 V. However, this voltage calculation takes into account only the peak voltage at the *fundamental* frequency. The square-wave current pulse delivered by the switched output devices is presented with a considerably different load impedance at harmonic frequencies; the resulting harmonic voltage components may add to the fundamental to result in a somewhat larger peak drain voltage than that calculated above. Therefore, it may be prudent to allow for a slightly greater voltage headroom, if flatness of power vs. VDD is a design goal.

As the output power is theoretically a function of only I_{PA} and R_{LOAD_INT}, the output power should not vary with changes in supply voltage as long as I_{PA} remains at its programmed value. If greater tolerance against a reduction in supply voltage is desired, it would be necessary to select a lower target value for R_{LOAD_INT}; this would result in a lower peak voltage swing (at the expense of an increase in the required value of I_{PA} and thus overall current consumption of the chip).

The PA output devices operate as programmable switched current sources and, ideally, deliver square wave pulses of current to the load. The amplitude of these square wave current pulses is programmable through the properties PA_PWR_LVL at 0x2201 and PA_BIAS_CLKDUTY at 0x2202. The value of PA bias current per transistor unit finger (in increments of 10 µA) is configured by the OB[5:0] field in the PA_BIAS_CLKDUTY property, while the total number of enabled transistor fingers is configured by the DDAC[6:0] field in the PA_PWR_LVL property. The total amplitude of the square wave current pulse is the product of these two values. As an example, if the OB[5:0] field is set to 0x22 = 34d and the DDAC[6:0] field is set to 0x64 = 100d, the programmed amplitude of the current pulse is I_{BIAS} = 34.0 mA (34 x 10 µA per finger x 100 fingers). Since the amplitude of the current pulse is a product of two values, it is often possible to obtain the same bias current amplitude with different combinations of settings. Silicon Labs recommends using a nominal value of DDAC[6:0] = 0x64 = 100 fingers and then selecting OB[5:0] as required; this allows for both upwards and downwards adjustment range if fine tuning of the output power is required.

The previously-calculated value for I_{PA_PK} of 25.38 mA represented the required current amplitude at the fundamental frequency. This is not the same as the amplitude of the square wave current pulse configured through the OB[5:0] and DDAC[6:0] fields. The relationship between the amplitude of a 50% duty cycle square wave pulse train and the amplitude of its fundamental component may be found through Fourier analysis to be:

$$I_{BIAS} = 2 \times I_{PA\_PK} \times \left(\frac{\pi}{4}\right) = 2 \times 25.38 \text{ mA} \times \left(\frac{\pi}{4}\right) = 39.9 \text{ mA}$$

Equation 12.

This value of bias current could be obtained by setting OB[5:0] = 0x28 = 400 µA per finger and DDAC[6:0] = 0x64 = 100 fingers, for a total square wave current pulse amplitude of 40.0 mA. The average (dc component) of this 50% duty cycle current pulse is half of the amplitude: I_{BIASDC} = I_{BIAS}/2 = 19.95 mA.

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This analysis assumes a square waveform with 50% duty cycle. The duty cycle of the current pulse may be adjusted to other selected values through the CLK_DUTY[1:0] field in the PA_BIAS_CLKDUTY property. The analysis for other values of duty cycle is not discussed here.

3.1.4. Calculation of Required Z_{LOAD} at the TX Pin

It is desired that the PA output devices be presented with a purely-real load at the fundamental frequency (i.e., $Z_{TOTAL} = R_{TOTAL} + j0$). It is thus necessary to present a load impedance Z_{LOAD} at the TX pin that appears inductive, such that the inductive reactance cancels the internal shunt capacitance of the PA devices (C_{PA}). It is necessary to calculate the external load impedance that when placed in series with $L_{SERIES} = L_{BW} + L_{TRACE} \approx 2.9$ nH and then in shunt with $C_{PA} = 2.006$ pF results in $Z_{LOAD\_INT} = 90 + j0\ \Omega = R_{LOAD\_INT}$ (continuing our Si4461 design example at 915 MHz).

The required impedance value Z_{LOAD} to present to the TX pin may easily be determined through graphical means (e.g., Smith Chart) or through the use of the impedance transformation equation shown below.

$$Z_{LOAD} = Z_R + jZ_I = \left(\frac{G_{LOAD\_INT}}{G_{LOAD\_INT}^2 + B_{CPA}^2} \right) - j\left(X_{Lseries} - \frac{B_{CPA}}{G_{LOAD\_INT}^2 + B_{CPA}^2} \right)$$

Equation 13.

For our 14 dBm design example at 915 MHz, this may be calculated to be $Z_{LOAD} = 43.3 + j28.3\ \Omega$.

3.1.5. Transforming R_{ANT} into Z_{LOAD}

A simple two-element L-C match is thus required to transform the (assumed) 50 Ω antenna impedance to the calculated value of $Z_{LOAD} = 43.3 + j28.3\ \Omega$. The required component values are again found easily through use of a Smith Chart and are determined to be a shunt capacitor CM1 = 1.37 pF and series inductor LM1 = 7.9 nH. Standard 5% component tolerance values of CM1 = 1.2 pF and LM1 = 8.2 nH are considered sufficiently close, as shown in Figure 11.

If lower impedance required (for a flat Vdd characteristic) the LM1 can be reduced. To keep the ZLOAD_INT pure real at the internal TX pin slight increase of the CM1 is required: E.g. with LM1 = 5.6 nH and CM1 = 1.5 pF the resulted a ZLOAD_INT = ~64 Ω instead of the original ~90 Ω.

Figure 11. Simplified SwCurr Match for +14 dBm at 915 MHz

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3.1.6. Verifying Initial TX Performance

The next step is to verify the performance of this simple SwCurr match. The match of Figure 11 was constructed on an RF test card and characterized. The measured performance for OB[5:0] = 0x28 (400 µA per finger), and DDAC[6:0] = 0x64 (100 fingers) was:

2-Element Match						
LM1	CM1	DDAC	OB	V_{DD}	P_{OUT}	I_{DD}
8.2 nH	1.2 pF	0x64	0x28	1.80 VDC	11.02 dBm	28.93 mA
				2.10 VDC	11.72 dBm	30.51 mA
				2.40 VDC	12.08 dBm	31.71 mA
				2.70 VDC	12.23 dBm	32.62 mA
				3.00 VDC	13.02 dBm	33.48 mA
				3.30 VDC	13.27 dBm	33.65 mA
				3.60 VDC	13.44 dBm	33.81 mA

The measured output power of +13.27 dBm for VDD = 3.3 VDC was about 0.73 dB below the target output power of +14.0 dBm. After some bench investigation, the following reasons were discovered for the discrepancy:

- The PA output resistance (R_{PA}) in large-signal conditions is somewhat lower than the small-signal value measured in "3.1.1. Measurement of PA Shunt Output Capacitance/Resistance (CPA/RPA)" on page 28. This results in a greater value of P_{LOSS} and thus a lower output power.

- The measured PA bias current (through L_{CHOKE}) was slightly lower than the programmed value, due to some compression in large-signal conditions. This also resulted in lower-than-calculated output power.

The value of PA bias current was increased to OB[5:0] = 0x2D (450 µA per finger) to compensate for the additional loss.

2-Element Match						
LM1	CM1	DDAC	OB	V_{DD}	P_{OUT}	I_{DD}
8.2 nH	1.2 pF	0x64	0x2D	1.80 VDC	11.22 dBm	29.78 mA
				2.10 VDC	12.14 dBm	32.00 mA
				2.40 VDC	12.71 dBm	33.57 mA
				2.70 VDC	12.93 dBm	34.59 mA
				3.00 VDC	13.71 dBm	35.45 mA
				3.30 VDC	14.05 dBm	35.67 mA
				3.60 VDC	14.26 dBm	35.85 mA

There is some reduction in output power as the VDD supply voltage is reduced; this is in agreement with our expectation of voltage clipping at supply voltages less than VDD ≈ 2.8 to 3.0 V. As stated in "2. Summary of Matching Network Component Values" on page 6, the Si4461 SWC 13 dBm 868M board designed for flat Vdd characteristic has only 1.5dB drop in the 1.8–3.8 V supply voltage range. This is due to the fact that the impedance (ZLOAD_INT) is lower (~60 Ω).

The measured conducted harmonics for the 915M simplified SwCurr match example are shown in Figure 12.

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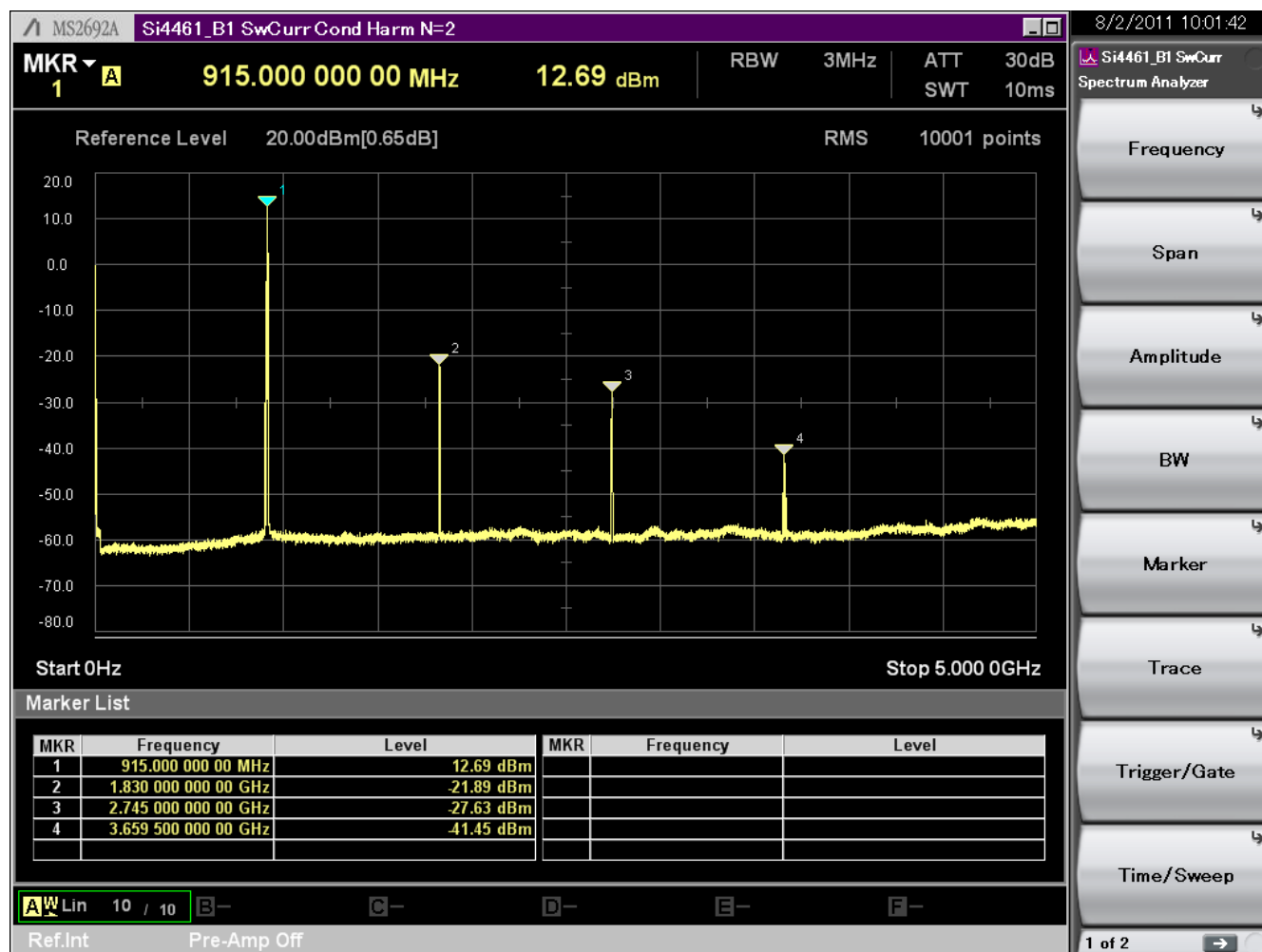
Figure 12. Conducted Harmonics for SwCurr Match at 915 MHz (N = 2)

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3.1.7. Adding a Low-Pass Filter

Although this initial measured performance is reasonable, the level of harmonics is unacceptably high. It is necessary to increase the order of the lowpass filter to reduce these harmonic signals to a level that is compliant with applicable regulatory standards (e.g., ETSI, FCC).

Theoretically, it should be possible to add more stages of lowpass filtering without modifying the impedance presented to the TX pin. If this is accomplished, then the only degradation in performance should be due to the insertion loss of the additional filter components.

The SwCurr match configuration that was built and verified in the previous section was only a 2nd order lowpass filter structure (CM1 and LM1). From experience on past designs (e.g., Si443x chips), it is expected that the required order of lowpass filtering to be N=3 to 4 (for ETSI) or N=4 to 5 (FCC). Continuing our design example at 915 MHz, a higher-order lowpass filter is now designed that also attempts to maintain the target load impedance of Z_{LOAD} = 43.3 + j28.3 ohms.

Using a graphical Smith Chart program (WinSmith™), a 4th order low-pass filter was designed. It should provide improved harmonic attenuation while theoretically transforming R_{ANT} = 50 Ω to Z_{LOAD} = 43.3 + j28.3 Ω. This low-pass filter was installed on our test board, and the performance was remeasured.

4-Element Match						
LM1	CM1	DDAC	OB	V_{DD}	P_{OUT}	I_{DD}
15.0 nH	5.1 pF	0x64	0x2E	1.80 VDC	11.03 dBm	28.92 mA
				2.10 VDC	12.11 dBm	31.65 mA
LM2	CM2			2.40 VDC	12.78 dBm	33.72 mA
12.0 nH	3.9 pF			2.70 VDC	13.13 dBm	35.06 mA
				3.00 VDC	13.93 dBm	35.99 mA
				3.30 VDC	14.24 dBm	36.29 mA
				3.60 VDC	14.39 dBm	36.51 mA

A reduction in output power level may again be obtained with this same match by simply reducing the PA output bias current field OB[5:0]. Output power levels of +13 dBm, +10 dBm, or 0 dBm may be obtained with a bias current of 390 µA per finger (OB = 0x27), 260 µA per finger (OB = 0x1A), or 70 µA per finger (OB = 0x07), respectively. Note that, as the voltage swing is reduced (as a result of lowering the unit bias current), the variation of output power as a function of supply voltage is also reduced. This is in agreement with theory. If it is desired to obtain less variation of output power vs. VDD at higher output powers (e.g. +14 dBm), it is necessary to redesign the match to target a lower value of R_{LOAD_INT} and increase the PA bias current accordingly.

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4-Element Match		DDAC	OB	V_{DD}	P_{OUT}	I_{DD}
LM1	**CM1**					
15.0 nH	5.1 pF	0x64	0x27	1.80 VDC	10.79 dBm	28.08 mA
				2.10 VDC	11.60 dBm	30.02 mA
LM2	**CM2**			2.40 VDC	12.05 dBm	31.48 mA
12.0 nH	3.9 pF			2.70 VDC	12.24 dBm	32.44 mA
				3.00 VDC	12.98 dBm	33.30 mA
				3.30 VDC	13.16 dBm	33.47 mA
				3.60 VDC	13.25 dBm	33.64 mA
		0x64	0x1A	1.80 VDC	9.34 dBm	24.50 mA
				2.10 VDC	9.59 dBm	25.22 mA
				2.40 VDC	9.69 dBm	26.08 mA
				2.70 VDC	9.75 dBm	26.86 mA
				3.00 VDC	10.14 dBm	27.59 mA
				3.30 VDC	10.20 dBm	27.70 mA
				3.60 VDC	10.25 dBm	27.82 mA
		0x64	0x07	1.80 VDC	0.27 dBm	15.12 mA
				2.10 VDC	0.13 dBm	15.80 mA
				2.40 VDC	0.10 dBm	16.68 mA
				2.70 VDC	0.08 dBm	17.46 mA
				3.00 VDC	0.27 dBm	18.12 mA
				3.30 VDC	0.31 dBm	18.22 mA
				3.60 VDC	0.34 dBm	18.33 mA

In practice, the value of PA output bias current is selected to nominally center the desired output power level. Further fine adjustment of the output power (upwards or downwards) may be accomplished by selecting a larger or smaller number of output device fingers (DDAC[6:0] field). The default value of DDAC used in the above measurements is 100 fingers (0x64). As the allowed range for this field is from 0 to 127 fingers, there remains room for upwards or downwards adjustment of the output power.

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The measured conducted harmonics for VDD = 3.3 V, OB = 0x2E (460 µA per finger), and DDAC = 0x64 (100 fingers) for the schematic of Figure 14 are shown in Figure 13 below. These conducted levels of harmonics now comply with the Radiated Spurious Emission requirements of FCC Part 15.205/209.
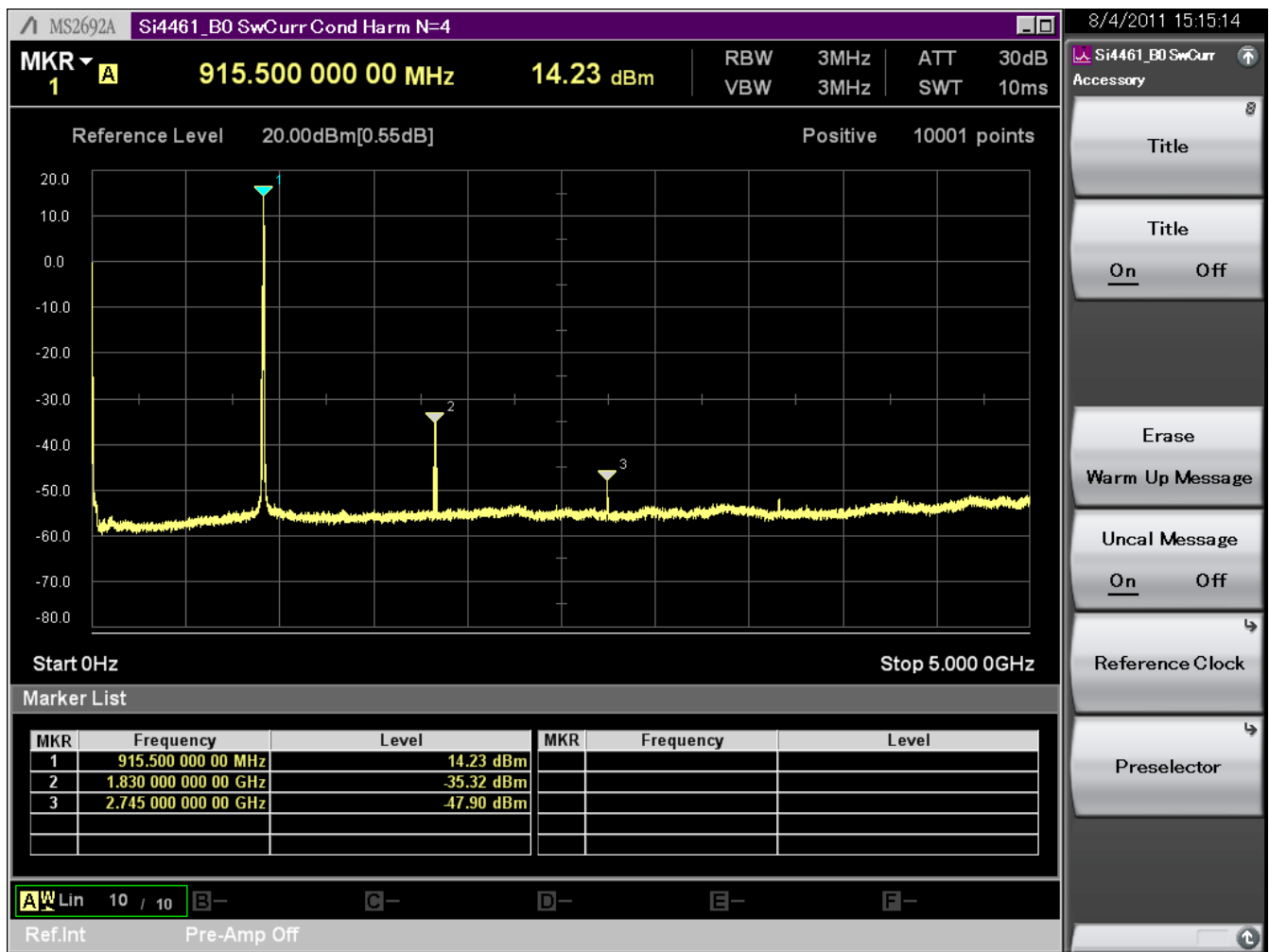
Figure 13. Conducted Harmonics for SwCurr Match at 915 MHz (N = 4)

3.1.8. Final Split TX/RX Schematic

The final schematic for a Split Si4461 TX/RX board Switched Current Match at 915 MHz for +14 dBm output power is shown in Figure 14 below.
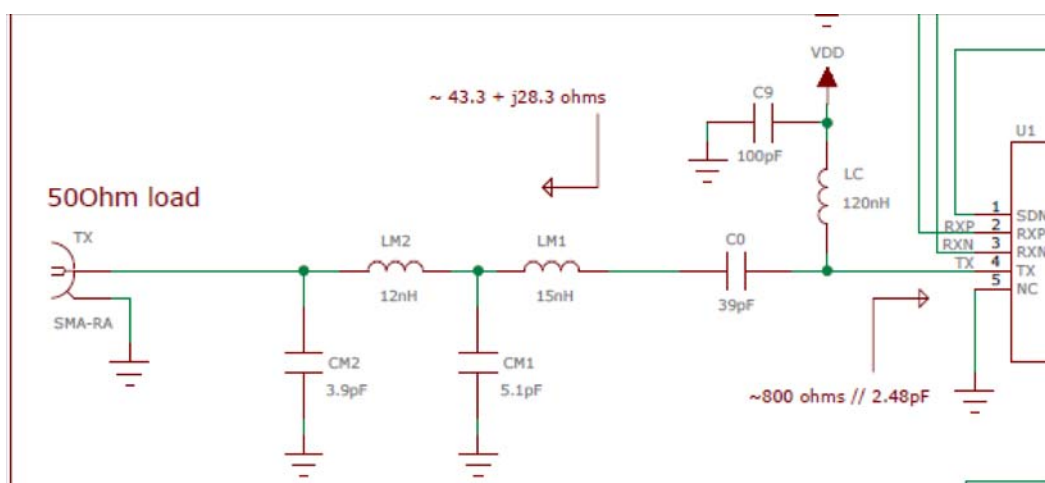
Figure 14. Final Schematic for Split SwCurr Match for +14 dBm at 915 MHz

3.1.9. Improved Efficiency at Lower Output Power Levels

As discussed in "3.1.2. Selection/Calculation of RLOAD_INT" on page 32, the selection of R_{LOAD_INT} is driven largely by the desired target output power level and the available VDD supply voltage. It is necessary to select a value of R_{LOAD_INT} such that drain voltage compression/clipping does not occur for the commanded output power level. If a lower output power level is desired, the value of R_{LOAD_INT} may be increased, thus requiring a lower value of PA bias current but providing improved current efficiency.

The design calculations and resulting component values shown in the previous sections assumed a target output power level of +14 dBm. If the desired output power level is reduced to (e.g.) +13 dBm, a higher value of $R_{LOAD\_INT} \approx 120~\Omega$ may be selected. In such a case, the design equations will result in the following parameters and component values:

- R_{TOTAL} = 109.3 Ω
- P_{LOSS_INT} = –0.41 dB
- I_{PA} = 14.2 mA (RMS fundamental), 20.0 mA (peak fundamental)
- I_{BIAS} = 31.4 mA → OB[5:0] = 0x20
- Z_{LOAD} = 41.15 + j40.29 Ω
- CM1 = 1.8 pF, LM1 = 11 nH

For the reasons discussed earlier, the initial measured output power for this design was again about 0.6 dB below the target output power of +13.0 dBm. The value of PA bias current was increased to OB[5:0] = 0x22 (340 µA per finger) to compensate for the additional loss, and the performance was remeasured.

2-Element Match						
LM1	CM1	DDAC	OB	V_{DD}	P_{OUT}	I_{DD}
11.0 nH	1.8 pF	0x64	0x22	1.80 VDC	10.46 dBm	25.91 mA
				2.10 VDC	11.08 dBm	27.15 mA
				2.40 VDC	11.46 dBm	28.29 mA
				2.70 VDC	12.03 dBm	29.50 mA
				3.00 VDC	12.51 dBm	29.99 mA
				3.30 VDC	12.85 dBm	30.15 mA
				3.60 VDC	13.05 dBm	30.30 mA

A significant improvement in current efficiency may be observed. For Si4060/4460/67 10 dBm SWC designs, the impedance should be even higher (~240 Ω for high efficiency target or lower if flatness is a concern).

3.2. Overview of Matching Procedure for SWC Direct Tie Board

In this section, the procedure for matching the Si4461 RFIC on an SWC Direct Tie (DT) board is discussed in detail. The procedure for the Si4460/67 chip is the same with different impedance and thus element values. The main steps in the matching procedure are summarized below:

1. Measure the typical PA shunt output capacitance (C_{PA}) and resistance (R_{PA}) of the chip.

2. Choose L_{CHOKE} (pull-up inductor) for high impedance at the desired frequency of operation.

3. Select/calculate internal load resistance R_{LOAD_INT} for the desired output power level.

4. Calculate PA bias current setting.

5. Calculate required external load impedance Z_{LOAD} to present to the TX pin.

6. Construct a simple 2-element L-C matching network to transform the antenna load impedance (typically R_{ANT} = 50 Ω) to the calculated PA load impedance Z_{LOAD}.

7. Add sections of low-pass filtering (while maintaining the desired impedance transformation ratio) necessary to attenuate the harmonic levels below the applicable regulatory standard.

8. Calculate the impedance at the common Direct Tie point in the TX=OFF state (i.e., RX mode).

9. Construct a standard four-element RX balun/matching network, assuming this value of impedance as the source impedance for the match.

10. Tie the TX and RX paths together at the common-impedance point, and verify that the performance of each path has not been significantly degraded.

A comparison of the above procedure with that shown in "3.1. SCW Matching Design for Split TX/RX Boards" on page 28 reveals that the first seven steps are identical. For either type of board configuration (Split TX/RX or Direct Tie), it is necessary to first construct a TX match. In the case of a DT board configuration, the RX match is added after the TX match has been designed.

3.2.1. Concept of Direct Tie Matching

In the Direct Tie board configuration, the TX and RX paths are tied directly together at a common point without the use of an RF switch. Careful design procedure must be followed to ensure that the RX input circuitry does not load down the TX output path while in TX mode and that the TX output circuitry does not degrade receive performance while in RX mode.

The RX input circuitry of the Si4461 and Si4460/67 chip contains a set of switches that aids in isolation of the TX and RX functions. This set of switches is implemented internally as shown in Figure 15.
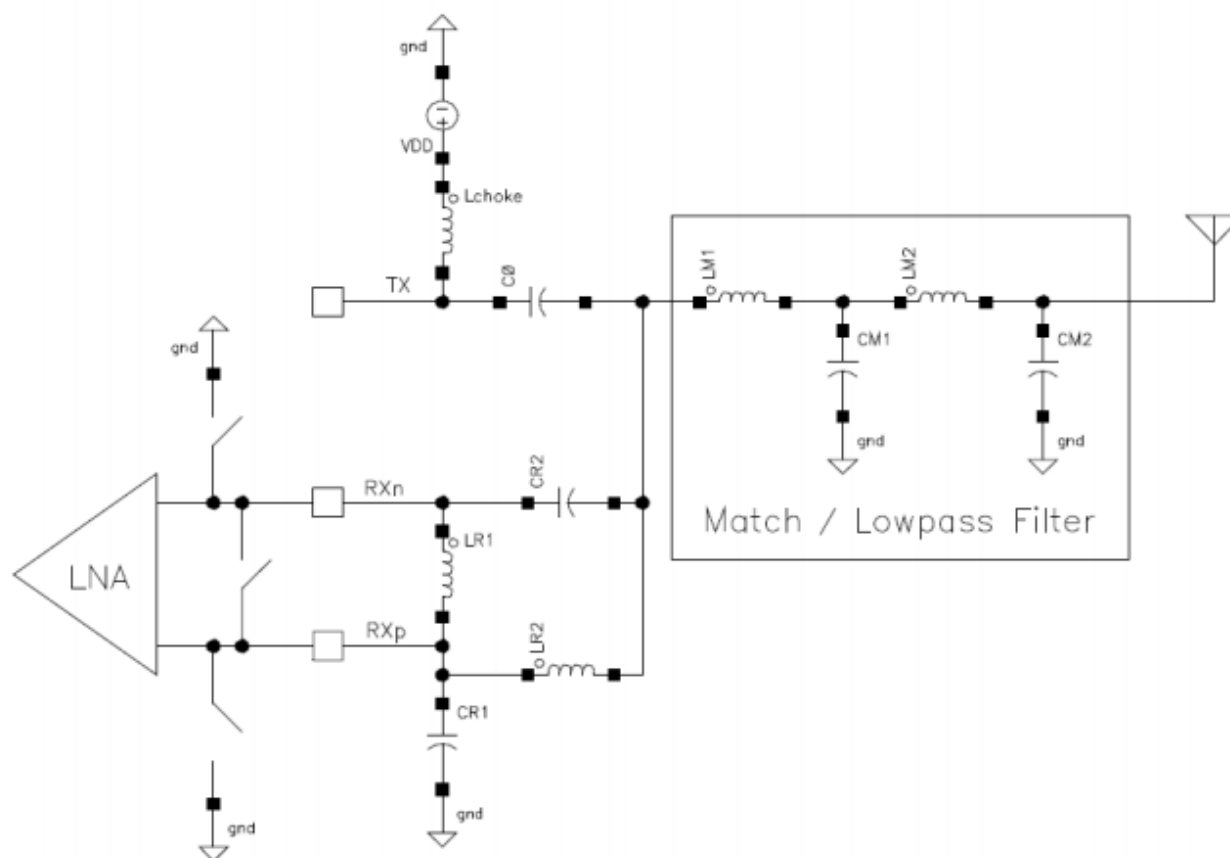
Figure 15. RX Input Switches for Direct Tie Operation

These three switches are activated and closed simultaneously upon entering TX mode; the switches remain open in all other modes, including RX mode. Closing these switches during TX mode effectively shorts the RXp and RXn input pins together and also shorts them to GND. The effective circuit may be redrawn as shown in Figure 16. Inductor LR2 and capacitor CR2 have effectively been placed in parallel by the closure of the switches and are connected to GND. If the values of these components are chosen for resonance at the desired operating frequency, a very high impedance is presented to the TX path resulting in very little degradation in TX output power. Also, by shorting the input pins of the LNA together and simultaneously to GND, the LNA is protected from the large signal swing of the TX signal. This feature allows connection of the TX path to the RX path without damage to the LNA.
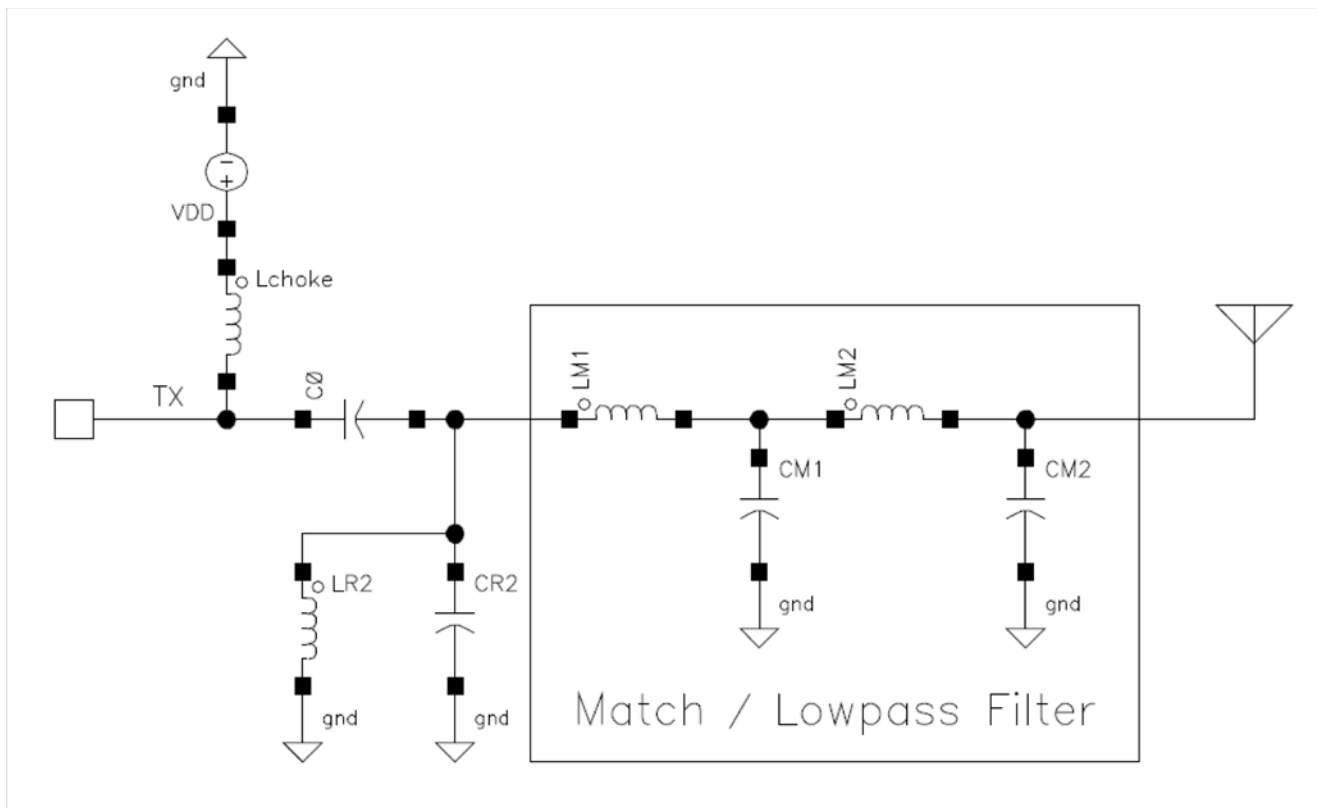
Figure 16. Effective Direct Tie Circuit in TX Mode

In RX mode, the output transistors of the PA are in the OFF state. However, the output impedance parameters of the PA (R_{PA} and C_{PA}) do not vary greatly between TX and RX modes. (The shunt output capacitance does decrease slightly in RX mode as compared to TX mode, but the decrease is only about 10%.) As a result, the output impedance parameters determined in "3.1.1. Measurement of PA Shunt Output Capacitance/Resistance (CPA/RPA)" on page 28 may be reasonably used in both TX and RX modes. The impedance of the pull-up inductor, L_{CHOKE}, is quite high and the impedance of the coupling cap, C0, is quite low, and both may be ignored for this discussion.

A key step in the DT matching procedure is to design/measure the impedance at the common direct tie point and to then construct the four-element RX match, assuming that impedance value as the source impedance. This common-point impedance is typically not exactly 50 Ω; however, there is nothing that prevents construction of an RX matching network for an arbitrary value of source impedance.

As discussed in "3.1.5. Transforming RANT into ZLOAD" on page 35, the impedance seen looking back into the match/low-pass filter network (i.e., looking back into LM1 with the chip disconnected) is equal to Z_{LOAD}. Additionally, connecting the TX pin of the chip results in placing the L_{SER}-R_{PA}-C_{PA} network in shunt to GND at this point, as shown in Figure 17. This modifies the source impedance presented to the input of the RX matching network away from the Z_{LOAD} value. While it is possible to express the resulting impedance mathematically in terms of Z_{LOAD} and the PA output impedance parameters, the resulting equation is rather unwieldy; it is much simpler to graphically determine the impedance on a Smith Chart.

The resulting impedance is reasonably close to being purely real and is close to (but slightly lower than) R_{LOAD_INT}. This is not unexpected; if the series bond wire/trace inductance (L_{SERIES}) was equal to zero, the resulting impedance would be *exactly* equal to R_{LOAD_INT}. A non-zero value of L_{SERIES} has an impedance-transforming effect that tends to lower the impedance observed at this point.
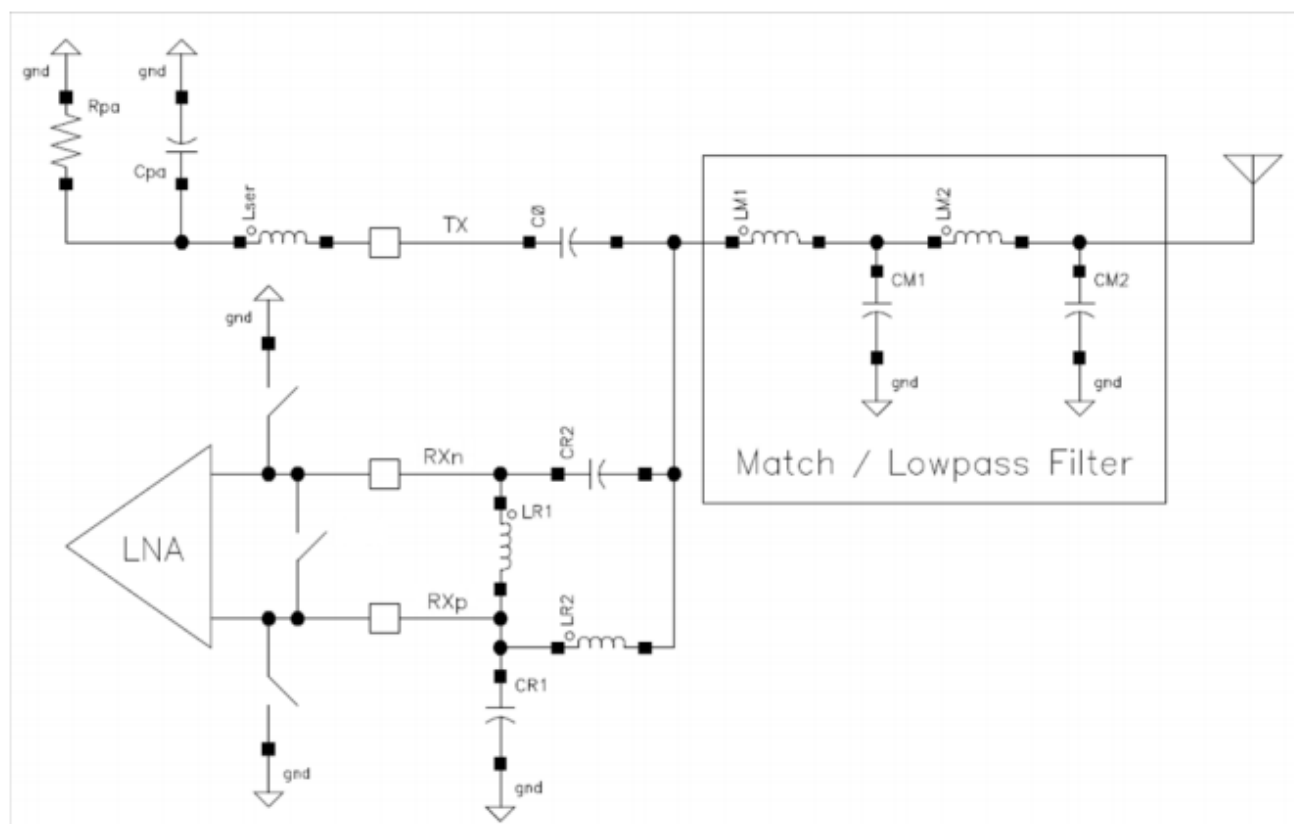
Figure 17. Effective Direct Tie Circuit in RX Mode

This (nearly) purely-real common impedance value now allows for a convenient tie-point that simultaneously satisfies the matching requirements for both signal paths. In TX mode, the RX matching network presents a high impedance and thus does not load down the TX signal. In RX mode, the R_{PA}-C_{PA}-L_{SERIES} network placed in parallel with Z_{LOAD} results in an approximately-real impedance that may be used as the source impedance for construction of the RX match. In this fashion, the performance of both signal paths may be maintained near their optimum levels (i.e., performance levels similar to those obtainable with a Split TX/RX board configuration).

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3.2.2. Construction of TX Match

The construction of the TX match (see Steps 1 through 7) is performed exactly the same as in "3. Switched Current (SWC) Matching Procedure Overview" on page 28 and is not discussed again here.

3.2.3. Calculate the Common Tie-Point Impedance

The circuit of Figure 18 may be analyzed to determine the source impedance presented to the input of the RX match in RX mode. This may done using graphical methods (e.g., Smith Chart) or with a basic circuit analysis program, such as SPICE. Continuing the Si4461 design example of 915 MHz, the impedance at this point is found to be ZSRC = 55 – j13 Ω. This impedance is sufficiently close to purely real to consider the common tie-point impedance to simply be RSRC = 55 Ω.
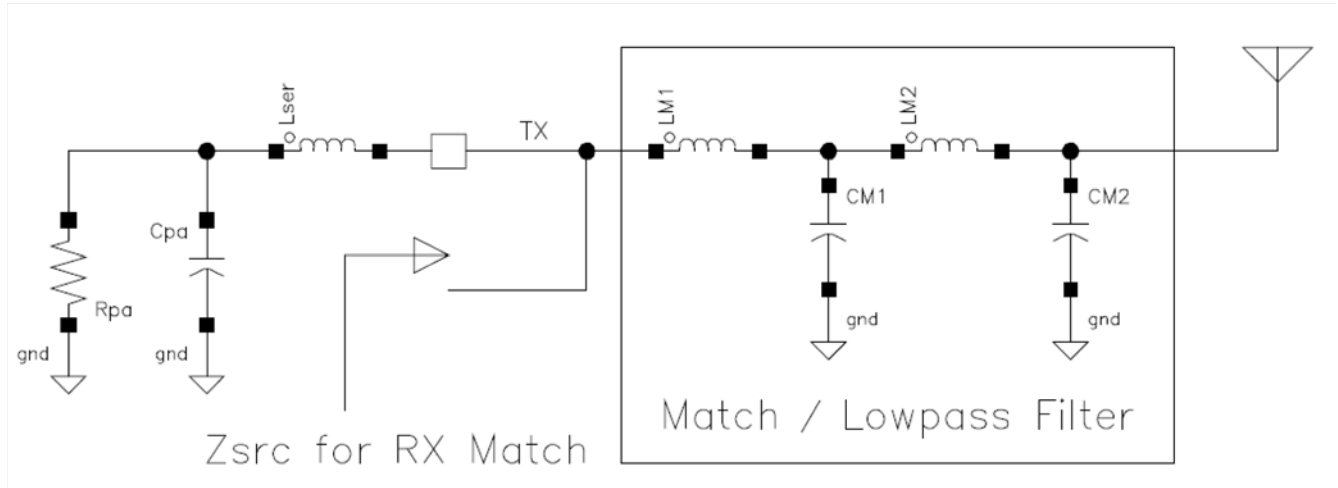
Figure 18. Equivalent Circuit of Source Impedance for RX Match

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3.2.4. Construction of RX Match

It is next necessary to construct a four-element RX matching network to simultaneously provide an impedance match as well as a single-ended-to-differential conversion function (i.e., balun). The mathematical derivation for the required component values has been thoroughly described in "AN643: Si446x/Si4362 RX LNA Matching"; the relevant equations from that document are shown here.

$$L_{LNA} = \frac{1}{\omega_{RF}^2 C_{LNA}}$$

Equation 14. .

$$L_{R2} = \frac{\sqrt{Re(Z_{ANT})R_{LNA}}}{\omega_{RF}}$$

Equation 15. .

$$L_M = \frac{2L_{R2}}{\left(\dfrac{2 \times Im(Z_{ANT})}{\omega_{RF}L_{R2}}\right) + 1}$$

Equation 16. .

$$L_{R1} = \frac{L_{LNA}L_M}{L_{LNA} + L_M}$$

Equation 17. .

$$C_{R1} = \frac{1}{\omega_{RF}L_{R2}}$$

Equation 18. .

$$C_{R2} = 2C_{R1}$$

Equation 19. .

In order to make use of the above equations, it is first necessary to know the LNA differential input impedance at the desired frequency of interest. This has been measured by Silicon Labs and is shown in Figure 19. The value of the RX input impedance is the same for both the Si4461 and Si4460/67. At 915 MHz, the input impedance is Z_{RX_LNA} = 48.8 – j109.4 Ω; the equivalent parallel input resistance and capacitance may be calculated to be R_{LNA} = 296 Ω and C_{LNA} = 1.33 pF.

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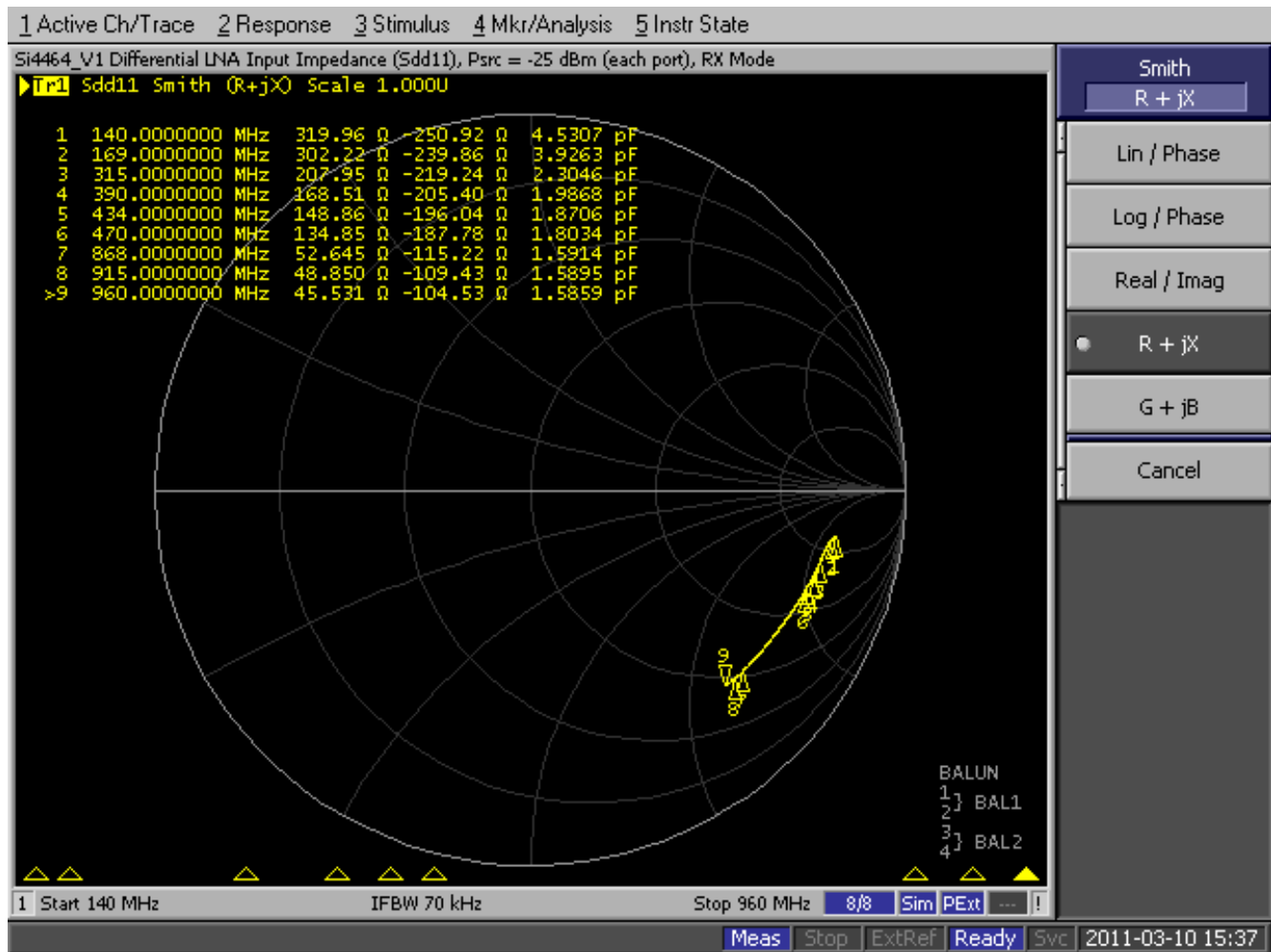
Figure 19. Si4461/Si4460/67 RX Differential LNA Input Impedance

The source impedance to which the RX input must be matched is the common tie-point impedance of Z_{SRC} = 55 Ω (in the 915 MHz Si4461 design example). Plugging the values of Z_{ANT}, R_{LNA}, and C_{LNA} into the above equations, the following calculated RX match component values are obtained:

- L_{R1} = 15.04 nH
- L_{R2} = 22.19 nH
- C_{R1} = 1.36 pF
- C_{R2} = 2.72 pF

These exact values may be rounded to the nearest-available 5% component tolerance values to arrive at L_{R1} = 15 nH, L_{R2} = 22 nH, C_{R1} = 1.3 pF, and C_{R2} = 2.7 pF. If desired, as an additional step of confirmation, this match may be constructed in a "stand-alone" configuration (i.e., not connected to the TX path) and its impedance measured. It was found that the input impedance and resonance were slightly off-target, likely due to parasitic trace and pad effects. The component values were adjusted slightly to optimize the impedance at the desired frequency.

- L_{R1} = 18 nH
- L_{R2} = 22 nH
- C_{R1} = 1.0 pF
- C_{R2} = 3.0 pF

The measured input impedance in RX mode for these component values is shown in Figure 20. The input impedance at the desired frequency of 915 MHz is 44 Ω; this is sufficiently close to the design target of 55 Ω.
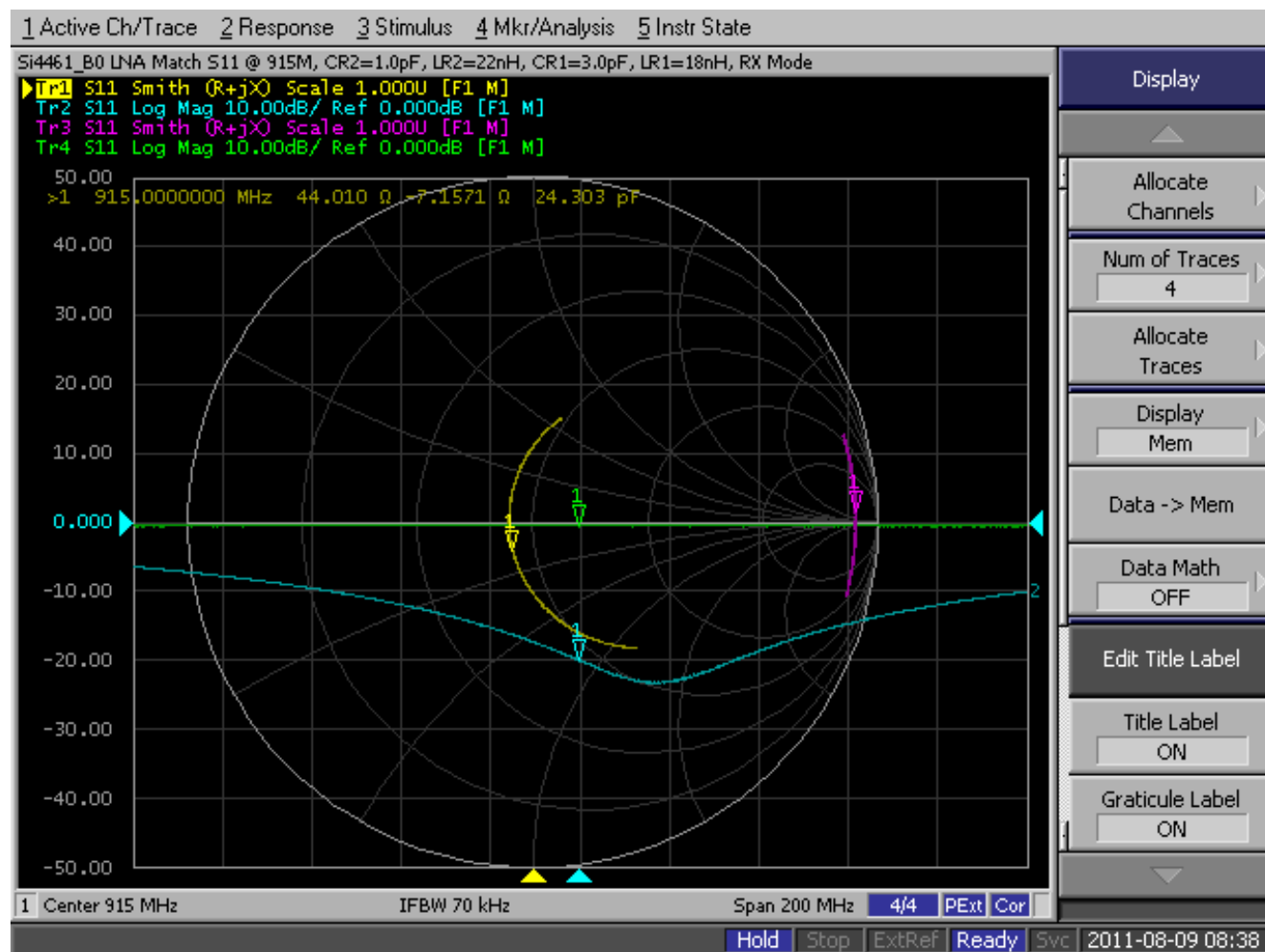
Figure 20. Si4461 SWC RX Match Input Impedance (RX and TX Modes)

It is also useful to verify the input impedance of this network in TX mode, when the LNA input pins are shorted together and also to GND. The input impedance of the match in TX mode is also shown in Figure 20 (magenta trace). It is seen that the circuit is nicely tuned to parallel-resonate at 915 MHz, thus presenting a very high impedance (~1.4 kΩ). This should allow the RX path to be connected to the TX path with very little degradation in TX mode.

3.2.5. Direct Tie Connection of TX and RX Paths

The next step is to actually connect the TX and RX paths at the common tie point (just after the series dc blocking capacitor). The TX and RX performance in the Direct Tie configuration is then remeasured.

The TX performance in Direct Tie configuration was measured as shown below.

2-Element TX Match						
LM1	CM1	DDAC	OB	V_{DD}	P_{OUT}	I_{DD}
8.2 nH	1.5 pF	0x64	0x2E	1.80 VDC	11.24 dBm	29.74 mA
				2.10 VDC	12.15 dBm	31.89 mA
				2.40 VDC	12.65 dBm	33.48 mA
				2.70 VDC	12.83 dBm	34.38 mA
				3.00 VDC	13.57 dBm	35.31 mA
				3.30 VDC	13.83 dBm	35.52 mA
				3.60 VDC	13.97 dBm	35.69 mA

Comparing with the previously-measured performance in Split configuration, the loss of output power is only ~0.2 dB! This is considered quite acceptable DT performance.

The RX sensitivity is also measured. The typical RX sensitivity performance in a Split configuration is known (from measurements on a large number of other boards) for 2GFSK DR = 40 kbps Dev = 20 kHz (h = 1) condition to be approximately –109.6 dBm for BER = 1E-3 (0.1%). The measured performance on this board in Direct Tie configuration is found to degrade by less than 1 dB. Again, this is considered quite acceptable performance.

4-Element RX Match				RX Sens (DR=40K Dev=20K)		
LR1	CR1	LR2	CR2			
18.0 nH	3.0 pF	22.0 nH	1.0 pF	Split =	-109.6 dBm	
				DT =	-108.8 dBm	

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3.2.6. Final Direct Tie Schematic

It is again necessary to add further stages of lowpass filtering in order to comply with the harmonic radiated spurious emission requirements of various regulatory standards, such as FCC or ETSI. The resulting final schematic for a Direct Tie board Si4461 Switched Current Match at 915 MHz for +14 dBm output power is shown in Figure 21.
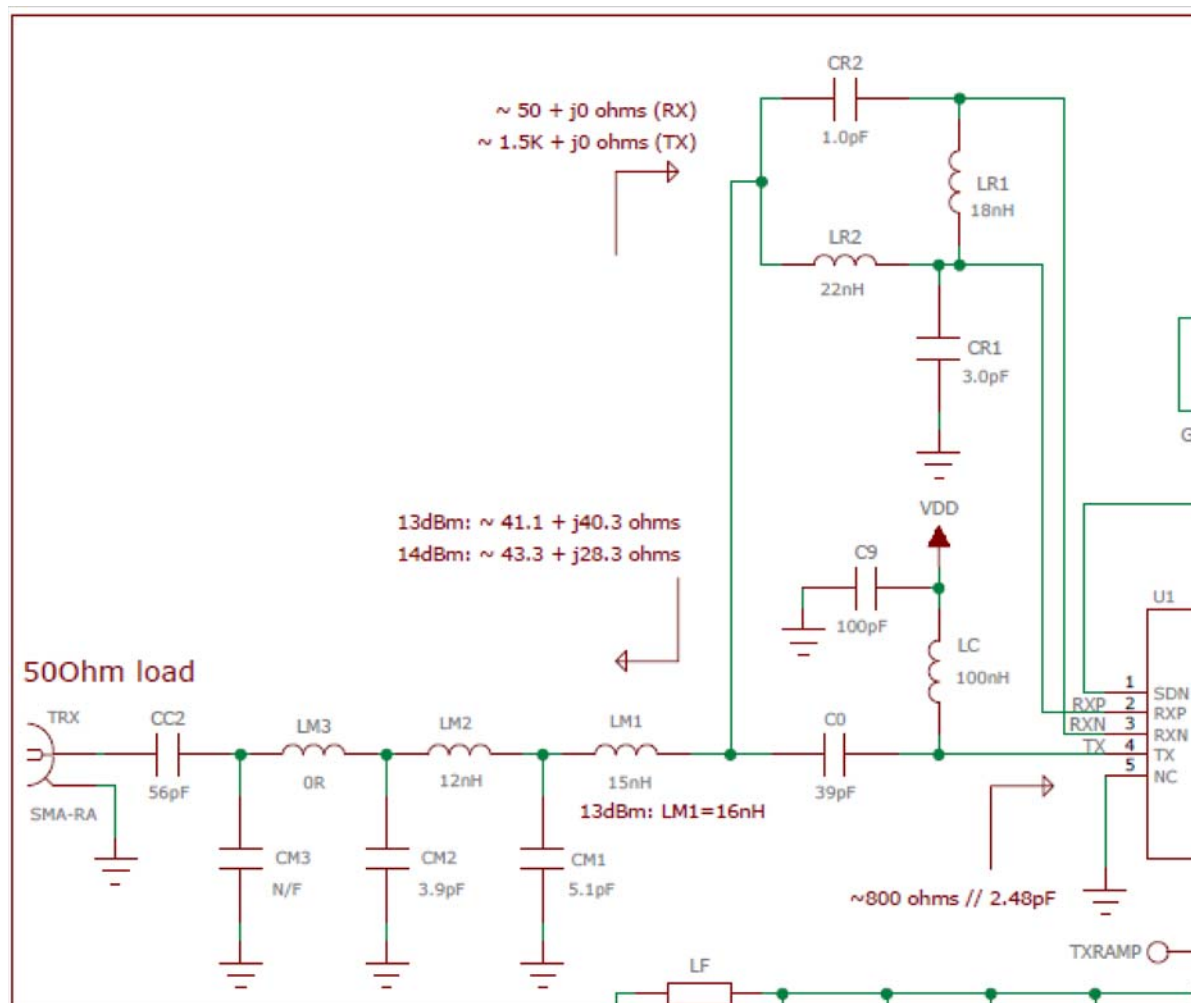
Figure 21. Final Schematic for Direct Tie Si4461 SwCurr Match for +14 dBm at 915 MHz

4. Class E (CLE) Matching Procedure Overview

Published matching procedures for well-defined classes of operation of switching amplifiers (such as Class-D or Class-E) may lead to operating conditions that exceed the maximum ratings (voltage or current) for the semiconductor process. As a result, we turn to a "customized" matching methodology that satisfies our desire for output power and efficiency while maintaining operation below the maximum voltage and current ratings for the RFIC. Note that this matching methodology is based upon Class-E theory but adds additional steps to aid in constraining the peak drain voltage. The drain voltage peak limit for long term reliable PA operation is 8 V in the case of the EZRadioPRO® family.

4.1. Brief Overview of CLE Matching Procedure

This application note discusses the CLE matching philosophy and procedure for the Si4060/Si4460/61/67 RFIC in great detail. However, some users may be interested in quickly gaining a high-level overview of the procedure before getting into the fine details. For those readers, the main points of the matching procedure are summarized below:

■ Choose L_{CHOKE} (pull-up inductor) for high impedance at the operating frequency, Fo.

■ Calculate the required value of Z_{LOAD} at the given Fo.

■ Calculate the required PA switcher loss for a given V_{DD} and desired output power. In the matchings applied here, instead of an external R_{DC}, the necessary loss is introduced by tuning the PA switcher FET loss (i.e with the PA power level setting).

■ Choose a value for C_0 (series capacitor).

■ Calculate L_0 (series inductor) and the required matching component values L_X and C_X.

■ Design a Chebyshev LPF (for attenuation of harmonics).

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4.2. Power Amplifier Circuit Description

RF design engineers are familiar with matching conventional (Class A/B/C) power amplifiers. In such cases, the matching procedure is relatively simple: provide a load impedance that is the complex conjugate of the output impedance of the PA. The reader may also employ Load Pull techniques in which a match is found that optimizes the output power but differs from the complex conjugate of the PA output impedance. In these conventional classes of power amplifiers, the output waveform ranges from a full 360 degree copy or reproduction of the driving waveform (e.g., Class A) to a partial (less than 360 degree) reproduction of the driving waveform (e.g., Class B or Class C).

However, the Class E type PA circuitry in the Pro family RFIC differs considerably from such a conventional power amplifier. Specifically, the PA circuitry in the Pro family is capable of working as a "switching power amplifier" or "switching power converter". The matching procedure for such a class of PA is entirely different and may not be immediately intuitive.

4.3. Basic Switching PA Circuit Topology

At the very heart of a switching PA is a switch. In the Si4060/Si4460/61/67, the switch is provided by group of NMOS transistors. Above the switcher FETs, a cascode stage with open collector output is used to increase the Vpeak allowed at the output. The number of bottom transistors can be tuned and sized to handle the current required for the specified output power.

- The higher-power Si4461 PA has 127 MOS switching fingers; so, the DDAC[6:0] field in the PA_PWR_LVL property register can go up to 7Fh. Its typical output capacitance is 1.9–2.2 pF, independent of the DDAC setting due to its cascode architecture.
- The lower-power Si4060/Si4460/67 PA has 79 MOS switching fingers; so, the DDAC[6:0] field in the PA_PWR_LVL property register can go up to 4Fh. Its typical output capacitance is 1.2–1.25 pF, independent of the DDAC setting due to its cascode architecture.

Figure 22 shows the basic class E matching circuitry necessary to extract RF power from a switching amplifier. In very general terms, the value of the pull-up inductor "L_{CHOKE}" is chosen to be a very large impedance at the frequency of operation (and its nearest harmonics), while the series-resonant output tank (L_0-C_0) is chosen to resonate at the frequency of operation. The shunt capacitance, C_{SHUNT}, is required to store energy during the switching cycle. This shunt capacitance, along with the extra series inductance, L_X, also works to tailor the time-domain shape of the output waveform. It is important to understand that, in order to optimize the efficiency of a switching-type amplifier, it is necessary to control the time-domain shape of the output waveform.
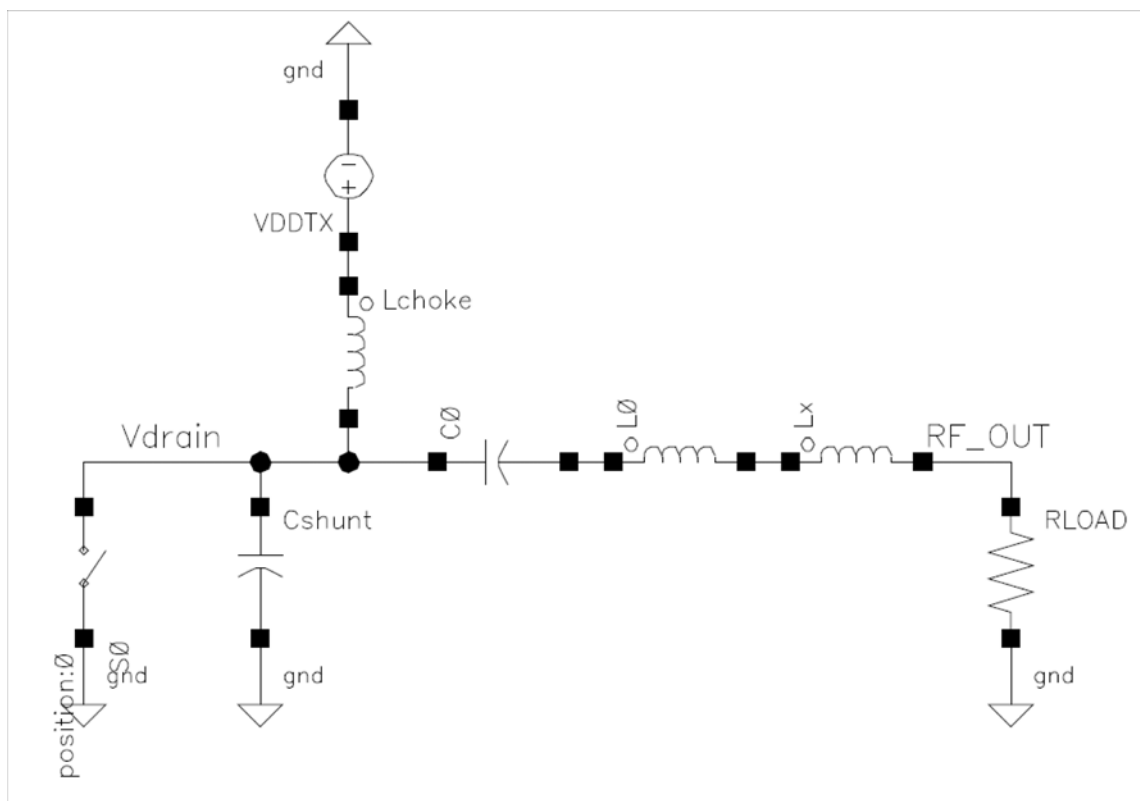
Figure 22. Basic Switching PA Circuit Topology

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4.4. Theory of Operation of an Ideal Switching PA

How does a switch "amplify" an RF signal? The simple answer is that it does not. As long as the input control signal to the switch is sufficient to toggle the switch between its ON and OFF states, the output waveform remains the same. Thus, the amount of output power delivered to the load resistance is independent of the amplitude of the input control signal (i.e., amplitude of the RF signal at the gate of the output MOS device); that is, a switching PA is a strongly nonlinear device. In such a case, defining the "gain" or amplification factor of the PA no longer has much meaning. Technically speaking, it is more correct to refer to this circuit as a "power converter" rather than a "power amplifier".

If the circuit does not amplify the internal RF input signal, what determines the level of the output power?

In an ideal class E switching PA, the level of output power is primarily dependent upon two parameters: the dc supply voltage and the shunt capacitance. This statement is interesting because, theoretically, there is no limit to the amount of power we can extract from a switching PA. Higher levels of output power can be obtained by either increasing the supply voltage or by increasing the shunt capacitance at the switching output device.

Furthermore, in an ideal switching PA, it is theoretically possible to achieve 100% efficiency. This is significantly different than conventional PAs. It is easily shown that the theoretical maximum efficiency of a Class-A PA is 50%, 78.5% for Class-B, and so on. However, in a switching PA, it is possible to tailor the output waveform such that the voltage across the switch is always zero during any period of time that the switch is conducting current, and the current conducted by the switch is always zero during any period of time that the voltage across the switch is non-zero. Thus, the power dissipated by the switching device itself is zero, and, in the absence of any other losses in the circuit, the efficiency approaches 100%. The theoretical voltage waveform at the drain of a switching amplifier operated in Class-E is shown in Figure 23.
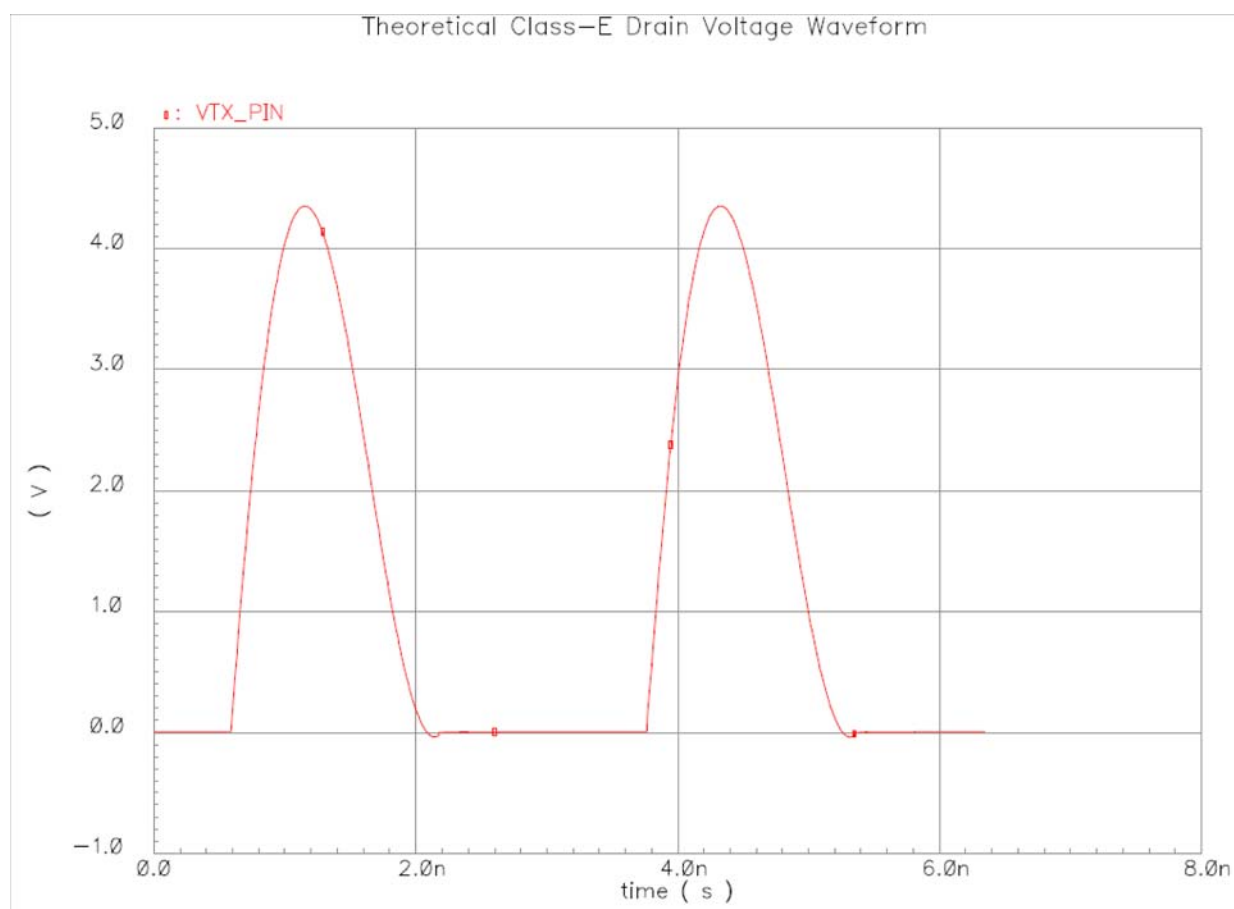
Figure 23. Theoretical Class-E Drain Voltage Waveform

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For those interested in learning more about the theoretical operation of switching amplifiers (especially Class-E amplifiers), the following papers are recommended:

- *Class E – A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers*, N. Sokal and A. Sokal, IEEE Journal of Solid State Circuits, Vol. SC-10, No. 3, June 1975.
- *Idealized Operation of the Class-E Tuned Power Amplifier*, F. Raab, IEEE Transactions on Circuits and Systems, Vol. CAS-24, No. 12, December 1977.

4.5. Limitations of a Practical MOS Switching PA

In practice, several factors prevent the "ideal" operation of a switching PA. These factors include the maximum operating voltage of the switch (i.e., MOS output device), the maximum current (limited by the size of the MOS output device), ON and OFF state resistances of the MOS output device, non-zero switching times of the MOS output device, and losses in the output matching components due to finite Qs. All of these factors combine to limit the achievable output power and efficiency.

The limitation on the maximum drain voltage of the MOS output device turns out to be a considerable constraint. RF design engineers may be quite familiar with the waveforms obtained with inductively-loaded conventional PAs, where the peak output voltage reaches a value equal to twice the dc supply voltage. However, the peak of the output voltage waveform in a switching PA may far exceed this "$2 \times V_{DD}$" rule-of-thumb. As is shown in the papers listed above, the peak drain voltage for a Class-E switching amplifier can reach 3.56 x V_{DD}.

The operational range of supply voltage for the Si4460/61/67 RFICs are specified as V_{DD} = 1.8 V to 3.6 V. It is apparent that, if the switching PA circuit was matched for Class-E operation at V_{DD} = 3.6 V, the resulting peak drain voltage would reach 12.8 V peak. This exceeds the maximum voltage at which the MOS devices (even in cascade configuration) can operate reliably without damage. As a result, at a higher VDD regime, the drain voltage must be constrained when matching the Si4060/Si4460/61/67 for Class-E operation. This is accomplished by introducing loss. It can be either a suitable choice of a limiting resistor R_{DC} in series with Lchoke, as shown in Figure 3, or it can be a properly tuned switcher loss. The matching procedure discussed in this application note takes care to constrain the peak drain voltage to a specified maximum value by proper tuning of the switcher loss.

Unfortunately, the introduction of any kind of loss causes a reduction in efficiency. One way to avoid this is to apply a dc-dc converter instead, which reduces the dc supply voltage properly at the Lchoke inductor. However, this method is usually too expensive for low-cost, short-range radio applications. Moreover, the switching noise generated by the dc-dc converter can cause several close-in mixing products in the TX spectrum. For these reasons, the introduction of loss remains the only low-cost way to limit the peak voltage at the PA's switching device drain.

The switching loss here can be modeled as a series resistance, which causes a dc voltage drop on the switcher; that is, with this loss, the PA supply voltage on the switcher output is decreasing. If the class E waveform is maintained, the allowed maximum of this PA supply voltage is Vpeakmax / 3.56 V = 8 V/3.56 V = 2.24 V since, for the cascode configuration to have reliable long-term operation, the maximum voltage rating of the semiconductor process is 8 V.

As mentioned earlier, in Class E operation, the output power at a given operating frequency is determined by the PA supply voltage and by the shunt capacitance at the drain of the switching output device. In the case of a real amplifier, where the PA supply voltage is decreased by the loss to limit the peak voltage, the shunt capacitance has to be increased to keep the targeted power. The increased capacitance results in a higher current peak and, thus, a higher dc current as well (since the peak current/dc current ratio is fixed ~2.56 in class E operation). That is, a real class E PA with tuned loss sacrifices efficiency to keep the 8 V peak voltage restriction at higher supply voltage levels.

Moreover, this is an optimized situation where the PA shunt capacitor value is adjusted to be close to the 8 V maximum peak limit at the operating frequency with the targeted power.

In real life, the PA capacitance is usually fixed. Especially at higher frequencies and lower power applications, it may happen that the capacitance value is larger than the optimum for 8 V peak voltage. In this case, the peak voltage (and thus the effective supply voltage on the switcher) is lower than the 8 V optimum; that is, a higher voltage drop, higher switcher loss, and higher power level back off must be introduced. Besides, due to the higher-value capacitor, the current peak (and thus the dc current) is also higher, which degrades the efficiency even more

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significantly. This is why a device with a higher PA capacitance value is not efficient in high-frequency, low-power applications (e.g. the Si4461 is not efficient at 868 MHz with +10 dBm power).

On the other hand, a device with an excessively low shunt capacitance value cannot achieve the targeted power with the 8 V voltage peak limit. To achieve the target power, a voltage peak higher than 8 V is necessary. Since it cannot be allowed again, switcher loss must be introduced. This is the reason why the lower capacitance device (e.g Si4060/Si4460/67) cannot achieve the +13 dBm level at low (169/315/434 MHz) frequencies even with wire-wound inductors (although, at 434 MHz, it is very close to that).

The calculation in "5.3.4. Step #4: Estimate the Required PA_PWR_LVL Register Value from the Calculated Value of a Voltage-Limiting Resistor" on page 62 helps to describe the situation even better.

The output capacitances and number of fingers of the Si4460/61/67 devices are sized in such a way that they can achieve the targeted normal operating power (i.e. 10 dBm in case of Si4060/Si4460/67 and 14 dBm in case of Si4461) at a wide frequency range with a strongly reduced power state at the typical 3.3 V external supply voltage level. Although, in this way, the RFICs sacrifices efficiency, it is still one of the best on the market at the time of this writing.

On the other hand, the reduced power state has many advantages, an important one being the improved robustness of the PA:

- The PA is less sensitive to load impedance variations. This is especially advantageous in battery-powered applications where any excess current increase of the RFIC (even a short one) caused by antenna impedance changes due to environmental condition variations significantly reduces the battery lifetime.

- There is room for power compensation with decreasing external supply voltage level (e.g. battery discharge) by simply increasing the number of switching fingers of the output device (i.e. by decreasing the switcher loss). Since the device has a built-in supply voltage detector, in theory, with a proper external MCU code, it can be adjusted automatically. Silicon Labs calls it "adaptive power control". Unfortunately, it is usually efficient only in the supply voltage range of 2.2 to 3.6 V.

The PA capacitance of the Si4060/Si4460/67 is 1.2–1.25 pF. With that, the IC can achieve 14 dBm at a maximum power state of 3.3 V V_{DD} at 868 MHz.

At lower frequencies (434/315 MHz), the capacitance value is too low, and, thus, the typical power the Si4060/Si4460/67 can deliver is only 12 to 13 dBm at 3.3 V V_{DD}.

The PA capacitance of the Si4461 is 1.9–2.2 pF. With that value, the maximum achievable power at 868 MHz is ~+18 dBm, while it is ~+17 dBm at ~434 MHz; so, here, there is a slight margin to use some back-off at the targeted 16 dBm power.

It must be emphasized that the given power values can be measured after the harmonic filter at the output SMA connector. The power at the class E tank output (before the filter) is approx 0.5 to 0.8 dB higher than that indicated with wire-wound inductors. With multilayer inductors, the power on the SMA is ~0.5 dB lower due to the higher losses (especially filter losses).

A good solution to have flat power and efficiency characteristics over a wide frequency range would be to use a tunable internal PA capacitance feature. However, since the achieved power and efficiency still meet the target (both at low and high frequencies), the simpler fixed PA capacitance method is used in the Si4060/Si4460/61/67.

5. CLE Matching Procedure for the Si4060/Si4460/61/67

This section provides a description of the Class E type switching mode matching process of the power amplifier (PA) on the Si4060/Si4460/61/67 family of RFICs. Specifically, this document does not address the matching procedure for the PA on the Si4063/Si4463/64/68 RFIC. Since the output power level on the Si4063/Si4463/64 RFIC is considerably higher than the Si4060/Si4460/61/67 RFIC, the matching procedure is somewhat different.

Also, due to the different power targets, the CLE matching network elements are quite different for the Si4060/Si4460/67 and Si4461. PA properties (basically the PA capacitance and the on-state FET loss), which primarily influence the achievable power, are different. In both chip versions, the maximum peak voltage should be lower than 8 V for long-term reliability.

The Class E matching design flow here is shown on the TX path of a split configuration. The special steps required for DT design (incl. RX path design) are summarized in "5.4. Detailed Matching Procedure for Direct Tie Board Configuration" on page 79.

5.1. Goals for the Matching Procedure

The matching methodology for the Si4060/Si4460/61/67 RFIC is aimed at achieving the following simultaneous goals:

- Basically, obtain +10 dBm (Si4060/Si4460/67) or 14 dBm (Si4461) of conducted RF output power even in DT configuration with multilayer inductors. In some bands, the Si4060/Si4460/67 can achieve 13 dBm, and the Si4461 can achieve 16 dBm.
- Constrain the peak drain voltage so that it does not exceed +8 V.
- Maximize efficiency on the PA output stage.
- Comply with ETSI and FCC specifications for spurious emissions.

These goals will be met under the following conditions:

- Operation at any frequency in the 169 – 960 MHz range.
- Antenna load impedance = 50 Ω.
- The chip is commanded to reduced power level mode (PA_PWR_LVL register is typically between 18h and 2Fh).
- Output power is measured at the matching output after the low-pass filter.
- Limitation on peak drain voltage are met for any V_{DD_RF} = 1.8 V to 3.6 V
- Si4060/Si4460/67 Output power of +10 dBm is met for V_{DD_RF} = 3.3 V (minimum) with less than 20 mA current or, in some bands, the power of +13 dBm with less than 25 mA current, even with multilayer inductors.
- Si4461 Output power of +14 dBm is met for V_{DD_RF} = 3.3 V (minimum) with less than 34 mA current or, in some bands, the power of +16 dBm with less than 45 mA current, even with multilayer inductors.

5.1.1. Comments on Peak Drain Voltage Limit

It should be noted that the +8 V peak drain voltage limit referred to above is not the same as the absolute maximum voltage rating at which the device may experience permanent damage. This absolute maximum voltage rating is higher than +12 V on the TX output pin.

Instead, this peak drain voltage limit of +8 V has been calculated as a limit, which, if not exceeded for continuous periods of time, should allow for multiple years of operation without noticeable degradation in output power. That is to say, if the peak drain voltage were to momentarily slightly exceed +8 V, the device would likely not be instantaneously damaged but might suffer a small decrease in long-term reliability.

In all cases, the voltage limit specified by the absolute maximum voltage rating should not intentionally be exceeded (however briefly) because instantaneous damage may occur.

5.1.2. Comments on Achieving the Targeted Output Power

This section is largely targeted at applications that require +10 dBm (Si4060/Si4460/67) or +14 dBm (Si4461) output power. While this level of output power is readily achievable, meeting other design constraints, such as harmonics, requires careful attention to matching component selection and good board layout techniques. That is

to say, it is possible to fail through poor design and poor board layout practices.

5.2. Matching Procedure Overview

5.2.1. Split TX/RX Board Configuration

The following steps provide a broad overview of the matching methodology for the Split TX/RX board configuration. Further details of each step will be provided later. The required design equations are discussed in "5.3. Detailed Matching Procedure for Split TX/RX Board Configuration".

1. First, select a value for the pull-up inductor, L_{CHOKE}, that provides a very large impedance at the frequency of operation (and its nearest harmonics).
2. Choose/calculate values for series-resonant tank, L_0-C_0, such that L_0-C_0 resonates at Fo.
3. Calculate the required value of Z_{LOAD} given the desired frequency of operation (Fo) and the known shunt drain capacitance of the Si4060/Si4460/61/67 chip ($C_{SHUNT60/61}$ = ~1.25/2.0 pF).
4. Estimate the necessary back-off of the power level setting. For this, calculate the required value for a hypothetical voltage-limiting resistor given the desired output power and main chip supply voltage, V_{DD_RF}. However, the calculated value does not used as an R_{DC} in series with Lchoke; instead, it is used to estimate the tuned switcher loss.
5. Calculate the values for the matching components, L_X and C_X, given the antenna load resistance (e.g., R_{ANT} = 50 Ω) and the calculated value for Z_{LOAD}.
6. Design a low-pass filter to provide sufficient attenuation of harmonic signals.
   a. The unfiltered waveform at the TX output pin will inherently contain high levels of harmonics.
   b. Depending upon the output power level and the desired level of harmonic attenuation, a third- to fifth-order low-pass filter will likely be required.

5.2.2. Single Antenna with Direct Tie Board Configuration

The following steps provide a broad overview of the matching methodology for the Single Antenna with Direct Tie board configuration. Further details of each step will be provided later. The required design equations are discussed in "5.4. Detailed Matching Procedure for Direct Tie Board Configuration" on page 79.

1. The same as the first step in the split match design (see "5.2.1. Split TX/RX Board Configuration")
2. The same as the second step in the split match design (see "5.2.1. Split TX/RX Board Configuration")
3. The same as the third step in the split match design (see "5.2.1. Split TX/RX Board Configuration")
4. The same as the fourth step in the split match design (see "5.2.1. Split TX/RX Board Configuration")
5. The same as the fifth step in the split match design (see "5.2.1. Split TX/RX Board Configuration")
6. The same as the sixth step in the split match design (see "5.2.1. Split TX/RX Board Configuration").
7. Construct a four-element match to the differential RXp/RXn input pins using the methodology outlined in "AN643: Si446x/Si4362 RX LNA Matching".
8. At 868/915 MHz, deliberately mis-tune the calculated value of L_0 downwards by approximately 20-30%. At 315/434 MHz, the split L_0 values usually work well.

5.3. Detailed Matching Procedure for Split TX/RX Board Configuration

In this section, we provide further detail about each step of the matching procedure for the Split TX/RX board configuration outlined above. We assume a general chip supply voltage of V_{DD_RF} = 3.3 V.

5.3.1. Step #1: Select a Value for L_{CHOKE}

In Step #1, we select an appropriate value for the pull-up inductor, L_{CHOKE}.

In the theoretical derivation for Class-E switching amplifiers, it is desired that the impedance of the pull-up inductor, L_{CHOKE}, be zero at dc and infinite at all other frequencies. This is not achievable in practice; however, a large value of inductance provides a reasonable approximation of this performance. The value of L_{CHOKE} should be chosen such that it provides a high impedance at not only the fundamental operating frequency but also at the first few harmonic frequencies. The inductance value should not be so large as to already be at (or past) parallel self-resonance at the desired operating frequency. The exact inductance value is not critical; however, Silicon Labs recommends the following range of inductance values (assuming 0402-size or 0603-size inductors) as a function of the desired operating frequency:

- 315 MHz: approximately 270 nH to 390 nH
- 470 MHz: approximately 220 nH
- 915 MHz: approximately 100 nH

With these inductance values, the self-resonant frequency is at least three times higher than the operating frequency.

5.3.2. Step #2: Choose/Calculate Values for the L_0-C_0 Series-Resonant Tank

In Step #2, we design the L_0-C_0 tank to be series-resonant at the desired operating frequency, Fo.

It is self-evident that there is an infinite number of combinations of L_0-C_0 values that can achieve resonance at a desired frequency. However, certain broad guidelines may be used to select one particular solution of component values.

First, it is desirable that the inductive and capacitive values be neither very large nor very small. Discrete inductors and capacitors with very large values are subject to degrading effects due to self-resonance. Discrete components with very small values are subject to greater degradation due to component tolerance. In either case, the actual resonant frequency of the tank may be significantly different than the frequency predicted by mathematical calculations.

Second, in the theoretical derivation for Class-E switching amplifiers, it is desirable for the impedance of the L_0-C_0 series-resonant tank to be zero at Fo and infinite at all other frequencies. This is not achievable in practice; however, a reasonable approximation of this performance may be obtained by using values with a high L-to-C ratio.

Third, it is desirable to minimize the insertion loss of the resonant tank. Since the quality factor (Q) of discrete inductors is generally much lower than that of discrete capacitors, it is important to select an L_0-C_0 ratio that maximizes the inductor Q. The Q of discrete inductors generally increases as the inductance value is increased until the inductance approaches the value where self-resonance becomes a concern.

Finally, it is desirable to select component values that are near standard 5% tolerance values. Unfortunately, this is rare in the case of multilayer inductors.

These considerations lead to the following guidelines for selecting the values for L_0-C_0:

- The L_0-C_0 tank must resonate at Fo.
- The value of L_0 should be chosen as large as possible (while remaining low enough for the effects of self-resonance to not be an issue and are close to standard 5% tolerance values).

In the present 868M design, we choose 3.6 pF as C0 and 9.3 nH as an L0 value.

5.3.3. Step #3: Calculate the Required Value for Z_{LOAD}

In Step #3, we calculate the required value of load impedance to be presented to the output of the L_0-C_0 resonant tank at the fundamental operating frequency, Fo.

In the theoretical derivation for Class-E switching amplifiers, it may be shown that the equations for output power (P_{OUT}) and load impedance (Z_{LOAD}) as a function of shunt drain capacitance (C_{SHUNT}) and supply voltage (V_{DD}) are as follows:

$$P_{OUT} = \pi\omega_0 C_{SHUNT} V_{DD}^2$$

Equation 20.

$$Z_{LOAD(fund)} = \left(\frac{0.2815}{\omega_0 C_{SHUNT}}\right) e^{j \times 49.0524°}$$

Equation 21.

These two equations are quite interesting. Equation 20 states that the theoretical output power is not a function of load impedance, but instead depends only upon the shunt drain capacitance (C_{SHUNT}), the desired operating frequency ($\omega_0 = 2\pi Fo$), and the PA supply voltage (V_{DD}). Equation 21 states that the required load impedance (Z_{LOAD}) does not vary with the desired level of output power but depends only on the desired operating frequency and the value of shunt drain capacitance.

The value of shunt drain capacitance, C_{SHUNT}, is a design parameter of the Si4060/Si4460/61/67 RFICs and is not adjustable by the user. This shunt capacitance is composed primarily of the drain-source capacitance, C_{ds}, of the output MOS cascade devices in parallel with a small amount of explicit integrated capacitance. Silicon Labs states that the value of this shunt drain capacitance is approximately:

$$C_{SHUNT} = 2.0 \text{ pF for Si4461 and } C_{SHUNT} = 1.25 \text{ pF for Si4060/Si4460/67}$$

These values may be substituted in the equations above and used to calculate other matching parameters. Assuming a desired operating frequency of Fo = 868 MHz as an example, the following value for Z_{LOAD} may be calculated, e.g., for the Si4060/Si4460/67:

$$Z_{LOAD(868M)} = \left(\frac{0.2815}{2\pi \times 868M \times 1.25 \text{ pF}}\right) e^{j \times 49.0524°} = 27.06 + j31.18\Omega$$

Equation 22.

This is the value of load impedance (at the fundamental operating frequency) that must be presented to the output of the L_0-C_0 resonant circuit.

It should be clearly understood that this value of load impedance (Z_{LOAD}) discussed above and the antenna impedance (Z_{ANT}) are not the same parameter nor do they necessarily have the same ohmic value. Given the arbitrary impedance of the antenna, one of the next tasks is to construct a matching network that transforms Z_{ANT} into Z_{LOAD}, as seen at the output of the L_0-C_0 resonant circuit.

5.3.4. Step #4: Estimate the Required PA_PWR_LVL Register Value from the Calculated Value of a Voltage-Limiting Resistor

In Step #4, we estimate the necessary power back-off, i.e. the DDAC field value of the PA_PWR_LVL register required for the desired output power. For this, the calculation of a hypothetical voltage-limiting resistor (not used directly in the circuit as R_{DC}) is required for a given specified value of PA supply voltage (V_{DD}).

Equation 20 clearly shows that, for a given desired operating frequency, the only "knob" remaining to the user to select the output power is the PA supply voltage, V_{DD}, since the value of C_{SHUNT} is an internal chip design parameter and is not adjustable by the user. Equation 20 is easily solved for V_{DD}, which is found to be:

$$V_{DD} = \sqrt{\frac{P_{OUT}}{\pi\omega_0 C_{SHUNT}}}$$

Equation 23.

Continuing our design example at 868 MHz and assuming a desired output power of +13.7 dBm (~23.4 mW) to compensate the losses and get ~13 dBm after filtering, the required value of V_{DD} may be calculated as:

$$V_{DD} = \sqrt{\frac{0.0234}{2\pi^2 \times 868M \times 1.25\ pF}} = 1.045\ V$$

Equation 24.

This equation states that, if the voltage supplied to the top of pull-up inductor L_{CHOKE} is equal to 1.045 V and the previously-calculated value of load impedance, Z_{LOAD}, is presented to the chip, the resulting output power will be P_{OUT} = 23.4 mW = +13.7 dBm at the class E tank output in an ideal, loss-free case.

This required PA supply voltage (V_{DD}) is significantly different than the general supply voltage (V_{DD_RF}) for the rest of the RFIC (e.g., for the VBATA and VBATD input pins). It is obviously not desirable to maintain two separate, independent sources of supply voltage for the RFIC; therefore, it is convenient to create the PA output supply voltage from the main supply voltage by means of an I-R voltage drop across a resistor.

This resistor can be either a series external one with Lchoke, as shown in Figure 3 on page 12 (R_{DC}), or an internal switcher loss. Although introducing the switcher loss instead of R_{DC} resistor results in a somewhat different operation, the final aim is achieved, i.e., the current flowing through on the switcher is limited, and, thus, the peak of the off-state voltage transient on Lchoke is reduced. The use of the internal loss instead of an external R_{DC} yields higher efficiency because, at significantly reduced power states, the previous internal PA drivers consume less current. Since the *theoretical* efficiency of an ideal Class-E switching amplifier tank is 100%, the average drain current, I_{DD}, may be calculated as:

$$P_{OUT} = \pi\omega_0 C_{SHUNT} V_{DD}^2 = I_{DD} V_{DD}$$

Equation 25.

This equation may be solved for I_{DD} to obtain:

$$I_{DD} = \pi\omega_0 C_{SHUNT} V_{DD}$$

Equation 26.

Given the main supply voltage for the remainder of the chip (V_{DD_RF}) and having previously calculated the required value of PA supply voltage (V_{DD}) and average drain current (I_{DD}), it is a simple matter to calculate the required value for R_{DC}:

$$R_{DC} = \frac{V_{DD\_RF} - V_{DD}}{I_{DD}}$$

Equation 27.

Continuing our design example at 868 MHz for +13.7 dBm class E tank output power, we calculate:

$$I_{DD} = 2\pi^2 \times 868M \times 1.25 \text{ pF} \times 1.045 \text{ V} = 22.4 \text{ mA}$$

Equation 28.

Assuming a general chip supply voltage of V_{DD_RF} = 3.3 V, we calculate:

$$R_{DC} = \frac{3.3 - 1.045}{0.0224} = 100.7 \ \Omega$$

Equation 29.

Theoretically, this value of resistance must be placed in series with L_{CHOKE} (if it is loss-free) in order to drop the general chip supply voltage down to the value required to obtain the desired output power. In actuality, due to losses at the operation frequency (e.g., Lchoke has significant losses on the order of 10 to 15 Ω, and there are other component losses as well), the required resistance value is lower.

This power is achieved at a Si4060/Si4460/67 DDAC field (of the PA_PWR_LVL register) value of ~34h with wire-wound inductors at 3.3 V. At this power setting, the switcher loss is approx ~88 Ω; so, together with the other losses, it is a realistic value.

5.3.5. Step #5: Calculate the Values for Matching Components L$_X$ and C$_X$

In Step #5, we calculate the values of the matching components required to transform the given antenna impedance, Z$_{ANT}$, into the required load impedance, Z$_{LOAD}$.

This matching effort may accomplished by simple and normal design methods, such as the Smith Chart or impedance matching CAD software (e.g., WinSmith™). Continuing our design example at 868 MHz and assuming an antenna impedance of Z$_{ANT}$ = R$_{ANT}$ = 50 Ω, we find that 50 Ω may be transformed to the required value of Z$_{LOAD}$ = 27.1 + j 31.2 Ω by shunt matching capacitance C$_X$ = 3.39 pF and series matching inductance L$_X$ = 10.26 nH. The resulting circuit topology is shown in Figure 23.

It should be noted that this is only one possible solution for the required impedance transformation; other matching topologies could have been used as well. The reader should also note that the required L$_X$-C$_X$ match topology depends upon the real part of the load impedance, Re(Z$_{LOAD}$). In this example, the real part of the load impedance was less than 50 Ω and thus an appropriate matching topology consisted of a shunt capacitor (C$_X$) and a series inductor (L$_X$). In the event that Re(Z$_{LOAD}$) had been greater than 50 Ω, an appropriate matching topology would have consisted of first a series inductor (L$_X$) followed by a shunt capacitor (C$_X$).

It is apparent that series inductors L$_0$ and L$_X$ in Figure 24 may be combined into one equivalent inductor with a value equal to the sum of their individual inductances in order to reduce parts count. This is a normal and usual practice.
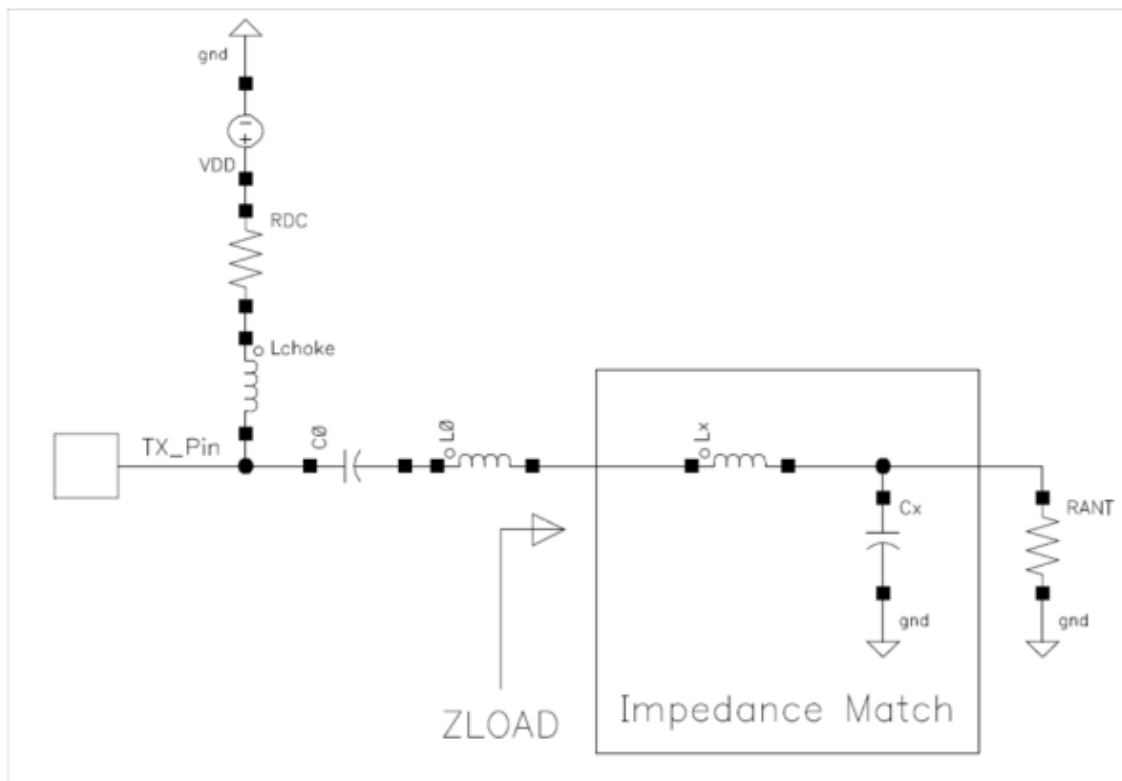
Figure 24. Impedance Match to Transform R$_{ANT}$ to Z$_{LOAD}$

5.3.5.1. Voltage Waveforms at TX Output Pin

At this point, the *basic* PA output match is complete. Although we have not yet designed a low-pass filter to sufficiently attenuate the harmonic signals, it is possible to measure the output power by substituting a power meter or spectrum analyzer in place of the antenna impedance, R_{ANT}.

It was previously mentioned that the peak of the drain voltage waveform in a Class-E switching amplifier may reach levels of $V_{PEAK} = 3.56 \times V_{DD}$. (This statement was offered without proof; for those readers interested in the derivation, refer to the papers listed in "4.4. Theory of Operation of an Ideal Switching PA" on page 55.) It is desirable to measure the actual drain voltage waveform in order to ensure compliance with our stated design goal of constraining the peak drain voltage to less than 8 Vpk.

It is not difficult to verify the resulting voltage waveform at the TX output pin (at least for the lower frequency bands of operation). A high-speed oscilloscope with an input bandwidth of at least 4 GHz (preferably higher) is required. A low-capacitance, high-bandwidth scope probe is also required, or, alternatively, the "resistive-sniffing" network of Figure 25 may be used. In this schematic, it may be seen that the inductors, L_0 and L_X, have been combined into one equivalent series inductance.
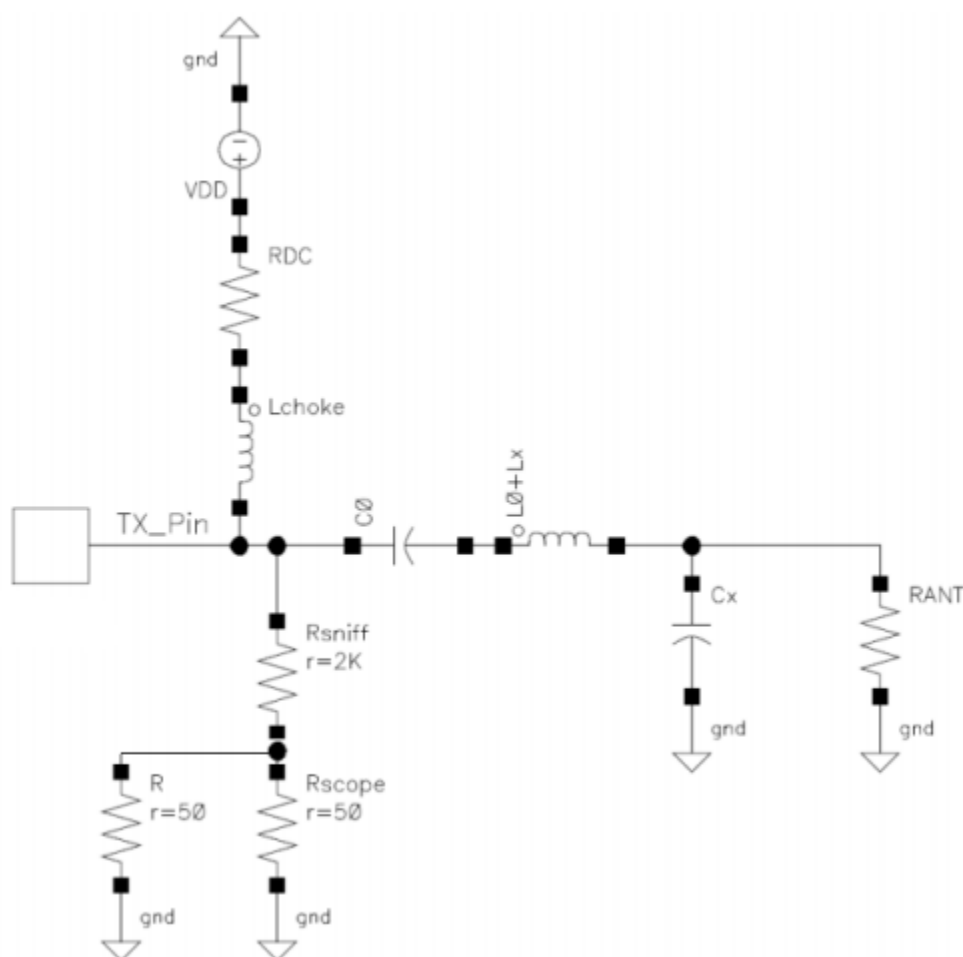
Figure 25. Resistive Sniffing Network

Using the "resistor sniffing" technique of Figure 25, the drain voltage waveform of Figure 26 was observed for an operating frequency of Fo = 868 MHz. In the example shown here, the following component values (obtained through use of the design equations above) were used:

- $P_{OUT(TARGET)}$ = +13.7 dBm
- VDD_RF = 3.2 V
- C_{SHUNT} = 1.25 pF (Si4460/67)
- L_{CHOKE} = 100 nH
- R_{DC} = 0 Ω
- DDAC value is 0x35
- C_0 = 3.6 pF
- L_0+L_X = ~19 nH
- C_X = 3.3 pF

The measured output power was +13.7 dBm at power state 0x35 at 3.2 V. The power state 0x35 required for the targeted power corresponds to approximately 86 Ω switcher on state loss. Together with the dc resistance of the Lchoke, it is approximately 88 Ω; so, the introduced loss is slightly lower than what is calculated by Equation 29. This is because the design equations above assume ideal switching operation of the output devices (i.e., zero ON-state resistance, infinite OFF-state resistance, zero switching time, etc.) as well as lossless discrete matching components. A practical switching amplifier and output match will inherently fall short of such ideal operation; some small degradation in output power is to be expected, which has to be compensated for by a slight increase of the PA power level setting (i.e further decrease of switcher on-state impedance). In any case, the difference is not significant.
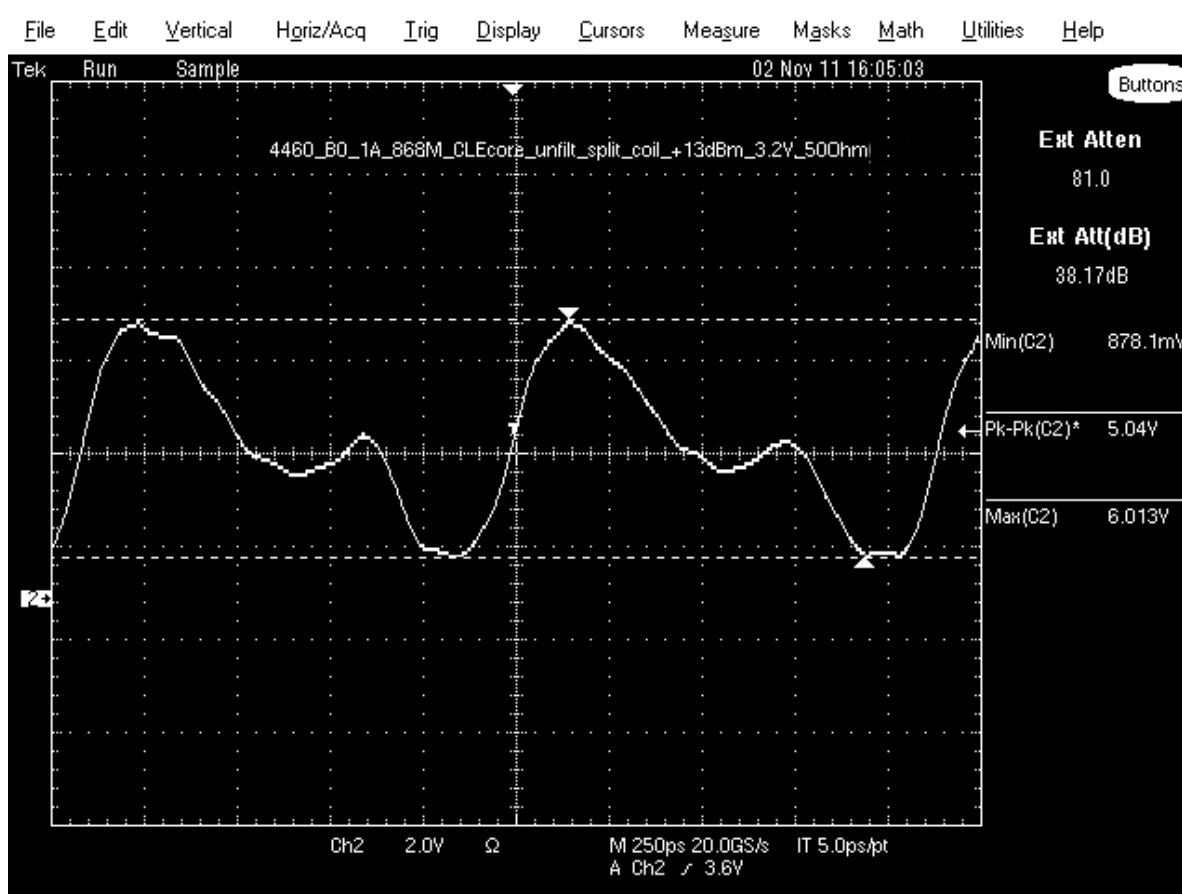
Figure 26. Drain Voltage Waveform (Fo = 868 MHz)

As can be observed in Figure 26, the measured waveform deviates to some extent from the theoretical "Class-E like" waveform at higher (868 MHz) frequencies. However, the maximum drain voltage is 6 V, much less than the critical 8 V.

It should be noted that the waveform would be closer to the theoretical Class E waveform at lower (315/868M) frequencies, as shown in Figure 27. As the operating frequency increases, it also becomes more difficult to faithfully observe the waveform. The input bandwidth of the oscilloscope used to display the waveform must increase in accordance with the operating frequency. Additionally, parasitic capacitances of the sniffing system and/or in the PCB layout as well as in the output device(s) of the RFIC tend to limit the high-frequency response of the amplifier.
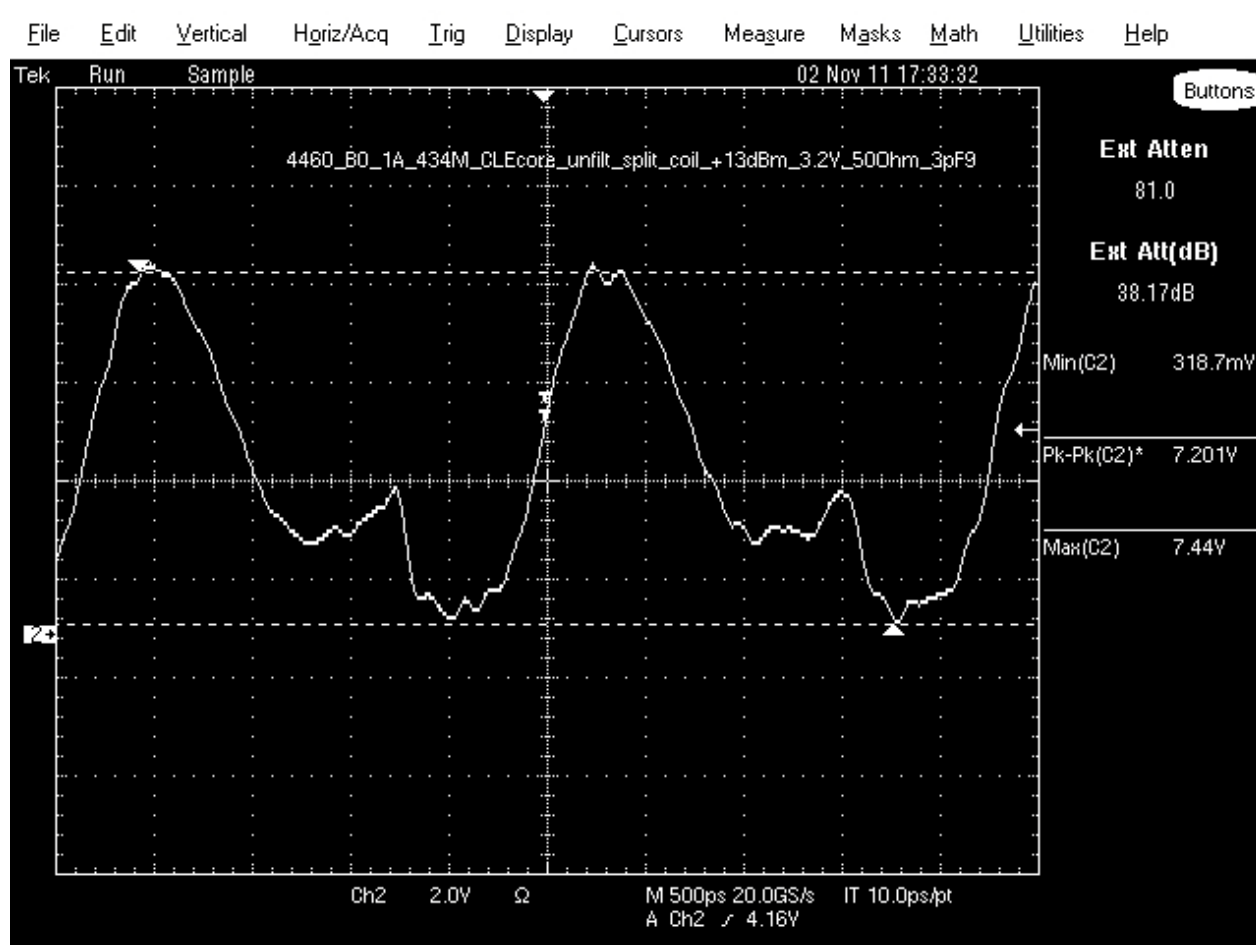
Figure 27. Drain Voltage Waveform of a 434 MHz Class E Tank

5.3.6. Step #6: Design a Low-Pass Filter

In Step #6, we design a low-pass filter network to attenuate the harmonics below the level required to meet applicable regulatory standards (e.g., FCC or ETSI).

5.3.6.1. Unfiltered Harmonic Spectrum

It should be understood that the waveform at the output of the match shown in Figure 24 will still contain relatively high levels of harmonics. Although the bandpass response of the series-resonant L_0-C_0 tank provides some attenuation of harmonic signals, it is generally not sufficient to meet applicable regulatory standards. This is normal for such a switching-amplifier and matching topology.

By way of example, the harmonic spectrum at the antenna load, R_{ANT}, for the matching network and component values of Figure 25 is shown in Figure 28 at power state 35h with 25.4 mA total current consumption at 3.2 V.
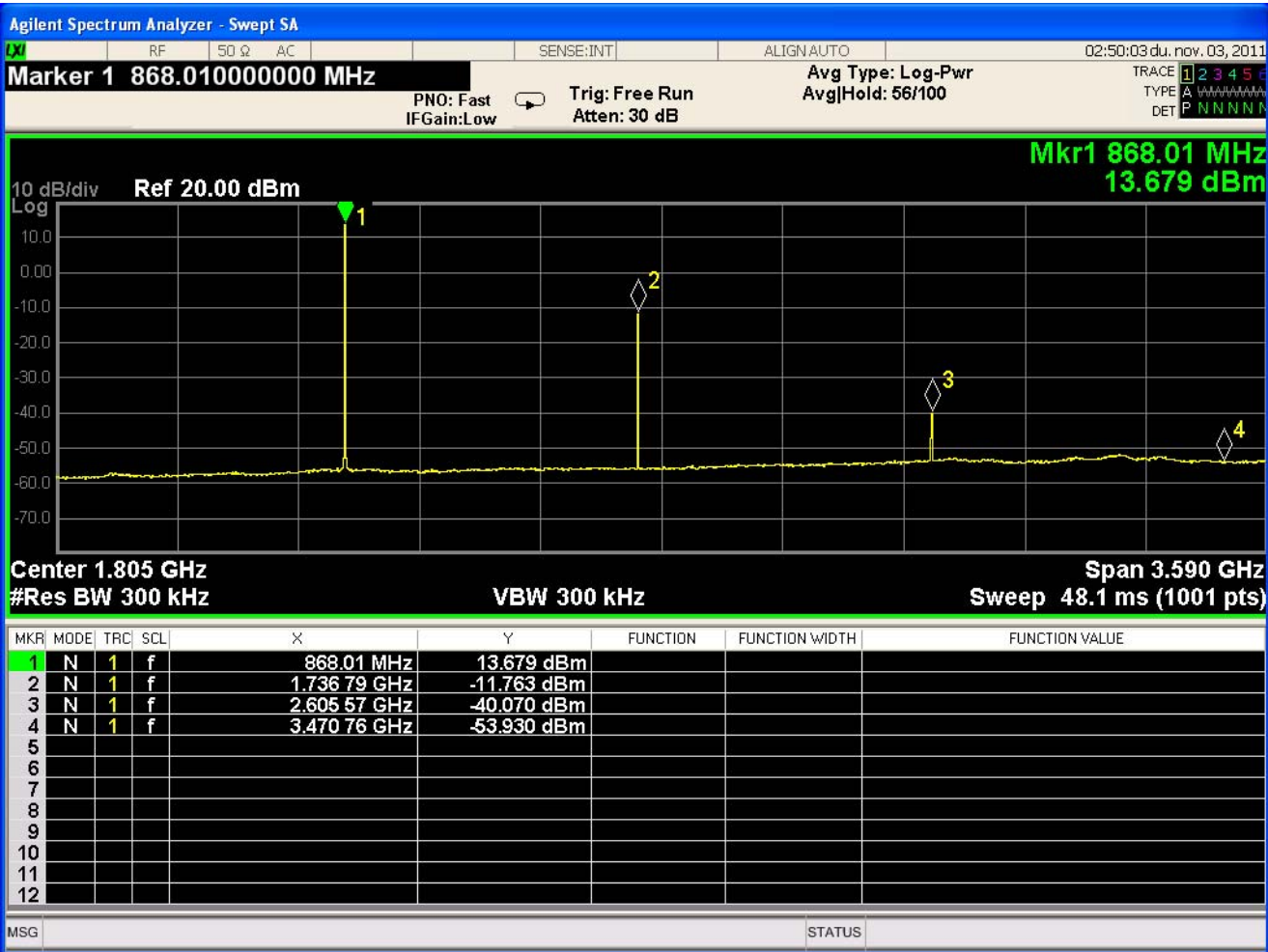
**Figure 28. Unfiltered Harmonic Spectrum at Power State 35h at 3.2 V
(Fo = 868 MHz, 25.4 mA Total Current)**

It must be noted that this Class E tank mainly uses the calculated values, assuming ideal loss and a parasitic-free case. As described earlier, in a real realization, there are losses, non-ideal switching characteristics, and several other parasitics, which degrades the operation with the calculated ideal values. Due to this, some bench tuning is usually useful to improve the performance. Although its mechanism is not fully clarified yet, a typical way to improve efficiency is to decrease the value of Cx (i.e., CM as it is denoted in "2. Summary of Matching Network Component Values" on page 6). In cases of strongly-reduced power (10 dBm Si4060/Si4460/67 design), the slight increase in C0 may also improve the efficiency. In any case, bench tuning/tweaking is always useful in the case of such a strongly nonlinear circuit.The following sections describe the final design with filtering.

5.3.6.2. Filtering Requirements

Since customers may operate under widely-differing regulatory standards, each with differing harmonic requirements, it is difficult for Silicon Labs to recommend one single low-pass filter design that is appropriate for all customers. However, a common regulatory standard that may be applicable to our design example at 868 MHz is ETSI Part EN300 220. This standard specifies the permitted levels of fundamental and harmonic frequencies in terms of Effective Radiated Power (ERP). The 868 MHz ETSI frequency band comprises several sub-bands with different properties. For example, the allowed power varies between +7 and +27 dBm with the most cases of 14 dBm ERP. At our desired operating frequency of 868.3 MHz (G1 sub-band), these maximum permitted ERP levels are:

- Fundamental = +14 dBm ERP
- Harmonics = –30 dBm ERP

Since the limits are specified in terms of ERP, compliance must be verified by measuring in an anechoic chamber with the unit operated into its intended antenna. The ERP is the power required to the input of an ideal dipole antenna with a gain of 2.14 dB to generate the same electric field at the far field. However, if an ideal isotropic antenna is assumed with 0 dB gain, higher conducted power is required at the antenna input by 2.14 dB. This equivalent level of conducted power is known as Equivalent Isotropic Radiated Power or EIRP.

Using EIRP limits, the equivalent conducted power ETSI limits are slightly higher:

- Fundamental = +16.14 dBm EIRP
- Harmonics = –28.86 dBm EIRP

It can be seen that the targeted +13 dBm power level with the Si4060/Si4460/67 is approx 3 dB lower than the fundamental EIRP limit of the ETSI; so, in theory, the gain of the applied antenna can go up to 3 dB. Unfortunately, in real applications, the typical monopole antenna gain is –5 to +2 dB, depending on many variables, such as available space, circuit dimensions (working as an electrical mirror ground plane), case, etc.; so, the ETSI fundamental limit is not approached in most cases. If operation close to the ETSI fundamental limit is required, Silicon Labs recommends the stronger Si4461.

On the other hand, the same antenna can became a good radiator at the harmonic frequencies where the antenna's relative size is longer and the same circuit (ground plane) dimensions give better electrical mirror properties, i.e. better radiation. It is especially true if the antenna impedance, varying strongly with frequency, causes acceptable reflection levels at these harmonic frequencies.

In any case, most of the antenna properties strongly depend on the actual antenna design and are difficult to predict in advance. Therefore, to have margin for a possible worst-case scenario, Silicon Labs usually defines the conducted harmonic levels to be 5 to 6 dB lower than the ERP limit; that is, in the case of 868 MHz operation, the harmonic levels should be below. ~–36 dBm.

5.3.6.3. Selecting a LPF Order and Type

Given the unknown radiation efficiency of every possible antenna selectable by the user, it is difficult for Silicon Labs to conclusively state the required filter attenuation characteristics. As a reasonable design compromise, the following design goals for the low-pass filter were settled upon:

- Minimal insertion loss at the desired operating frequency.
- A minimum conducted level of –36 dBm at all harmonic frequencies. Since the most critical second harmonic level is approx –8 to –10 dBm, the necessary minimum harmonic attenuation is approx 28 dB.
- The lowest filter order possible to still achieve this required harmonic attenuation.
- A 1:1 impedance transformation (i.e. 50 Ω input and 50 Ω output impedance).

Note that the amplitude characteristics in the lower portion of the passband of the LPF are relatively unimportant because the output signal contains no frequency components below the fundamental frequency. We are free to choose the filter type (e.g., Butterworth, Chebyshev, Elliptic) based primarily upon the filter's attenuation characteristics rather than its passband response.

A Butterworth filter design is not optimal because it provides relatively poor high-frequency attenuation characteristics; there is no need to sacrifice high-frequency attenuation in order to obtain a maximally-flat in-band frequency response.

Similarly, an Elliptic filter design (Cauer-Chebyshev) may provide insufficient attenuation at higher-order harmonic frequencies. While it may be possible (and advantageous) to tune a transmission zero in the stopband to the frequency of a problematic harmonic (e.g. N = 2 or N = 3), it is paid for with a decrease in attenuation at higher harmonic frequencies. As the unfiltered harmonic spectrum of Figure 28 shows, there remain several higher-order harmonics with significant energy that cannot be ignored and must be attenuated.

As a result, we settle on a Chebyshev low-pass filter design as an acceptable type of filter response.

With a Chebyshev filter, it is possible to obtain a greater rate of attenuation roll-off in the stopband by accepting a larger amount of amplitude ripple in the passband. The next issue to be addressed is the amount of passband ripple to be targeted in the filter design.

Greater attenuation at high frequencies can be obtained by employing a filter designed for a relatively large amount of passband ripple, but this trade-off should not be pushed too far. While a reasonable amount of passband ripple is perfectly acceptable, there is a limit to what can be considered reasonable.

Figure 29 shows the passband frequency response of an ideal (lossless) Chebyshev filter with 0.17 dB of amplitude ripple in the passband. It is quickly apparent that, in order to minimize the insertion loss of the filter at the desired operating frequency, it is necessary to design the cutoff frequency of the filter such that the desired operating frequency falls at one of the passband amplitude ripple peaks (Cursor "A" in the plot). If the filter cutoff frequency varies due to component tolerances, the filter response may vary such that the desired operating frequency falls on a minimum of the amplitude ripple response rather than on a maximum. In such a scenario, the filter insertion loss will increase, and the TX output power will decrease.

By designing for a limited amount of passband amplitude ripple, an upper limit is placed on the filter insertion loss due to mistuning of the component values. It is the opinion of Silicon Labs that a Chebyshev passband amplitude ripple of 0.15 dB to 0.5 dB represents a reasonable design trade-off between high-frequency stopband attenuation and potential passband filter insertion loss due to component tolerance.

As mentioned earlier, at 868 MHz, the filter attenuation should be at least 26 dB at the second harmonic frequency. To achieve this, at least a five-order filter is required with the targeted ripple level. Since the cost of an SMD capacitor is usually much lower than that of an SMD inductor (even though they are multilayer ones), it is advantageous to chose a filter structure in which the filter starts with a parallel capacitance (PI topology).

As usual, the SMD inductors, especially the multilayer ones, have much lower Q than the SMD capacitors; the lower number of series inductors is also advantageous since the extra attenuation caused by the losses is lower.

S21[dB] Ideal 5th order Chebyshev response with 20% passband reflection and 908.6M cuttoff
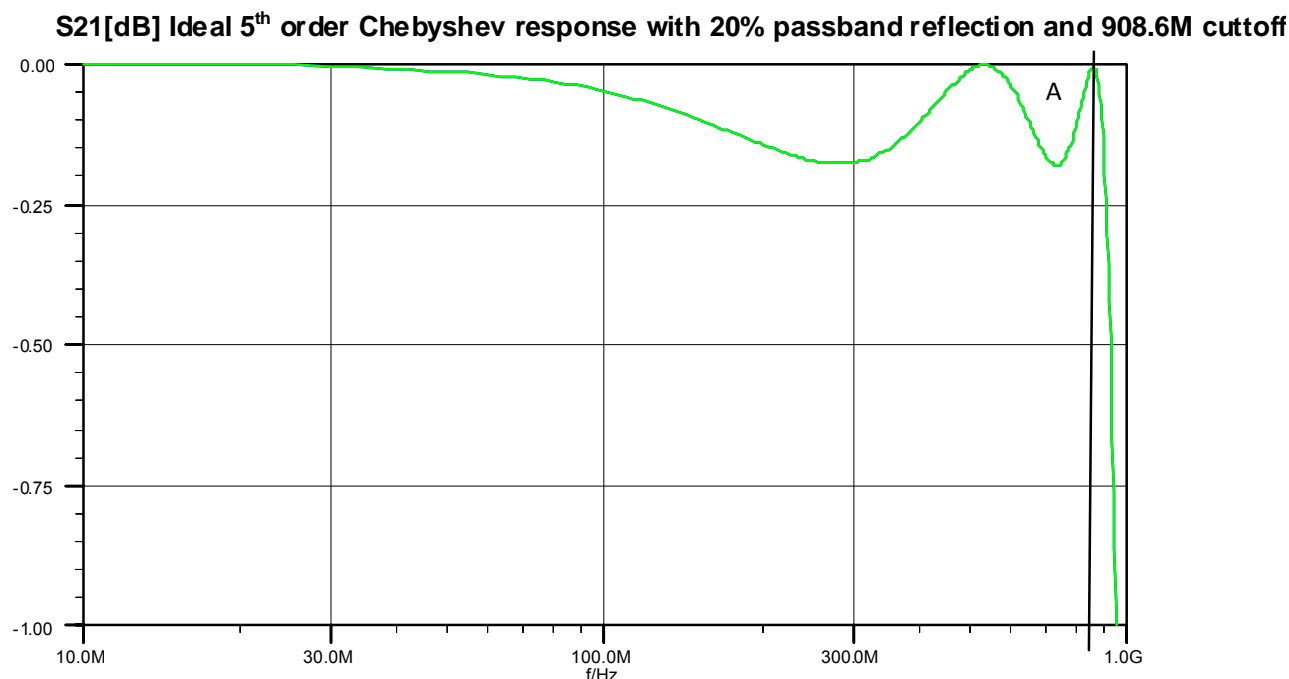
Figure 29. Ideal 5th-Order 0.17 dB Ideal Chebyshev Filter Response at 868 MHz

5.3.6.4. Calculation/Design of Component Filter Values

Actual filter component values may be obtained by the usual design methods, such as Filter Design CAD software or tables of normalized filter values scaled to the desired frequency of operation.

Due to the attenuation margin of the fifth-order design and the extra loss introduced by the losses, a slightly lower ripple prototype is chosen here: T520, that is, the maximum passband voltage reflection is 20%, which corresponds to approximately 0.17 dB ripple in a loss-free case.

The possibility of a fourth-order filter was also investigated, but, with that, the highest attenuation at the second harmonic is around 28 to 29 dB, that is, at the edge without loss parasitics. In order to have margin and also decrease the insertion loss (i.e. achieve better attenuation with lower passband loss) the fifth-order filter was chosen. Moreover, the fifth-order filter uses only one more capacitor, which is a very low-cost element.

Note that Silicon Labs recommends designing the filter such that the desired operating frequency falls at a peak of the amplitude ripple response rather than at the 3 dB cutoff frequency or at the equal amplitude ripple cutoff frequency (F_{ERCUT}). In this manner, the insertion loss of the filter will be minimized, and the TX output power will be maximized. For a fifth-order 0.17 dB Chebyshev filter, the ratio of FERCUT to FPEAK is approximately 1.0468:1. That is, if the desired operating frequency is 868 MHz, the filter must be designed for an F_{ERCUT} of 868 x 1.0468 = 908.6 MHz.
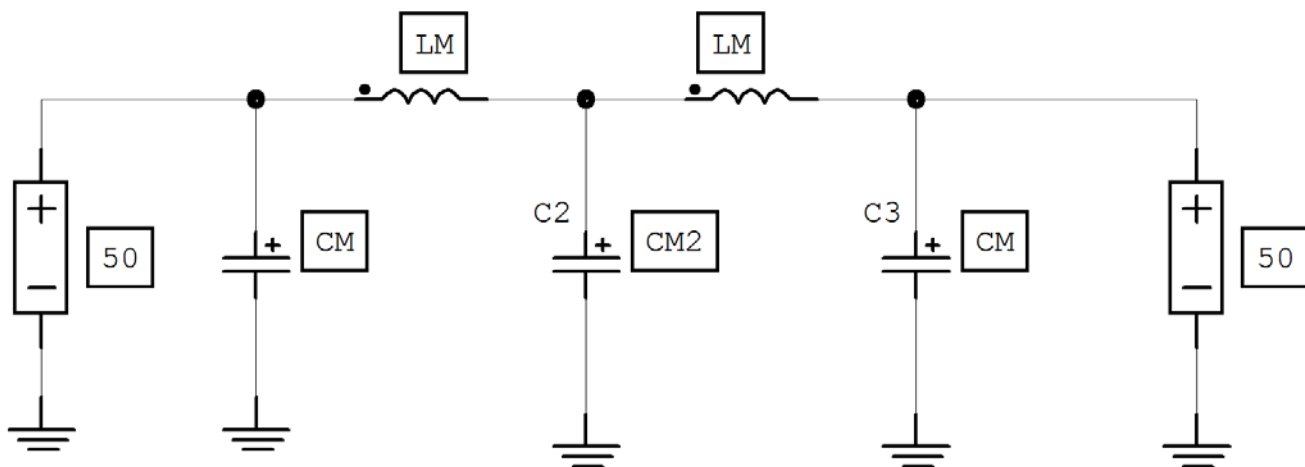
Figure 30. 3rd-Order PI-Topology Low-Pass Filter

Figure 30 shows the general architecture of a fifth-order, low-pass filter using the PI-topology. After design of a 0.17 dB ripple Chebyshev filter with a peak frequency of 868 MHz (F_{ERCUT} = 908.6 MHz), the following component values are obtained between 50 Ω termination impedances:

- CM = 4.561 pF
- LM = 11.79 nH
- CM2 = 7.458 pF

It is generally sufficient to use the nearest available standard 5% component tolerance values. Making these substitutions results in the following set of component values:

- CM = 4.7 pF
- LM = 12 nH
- CM2 = 7.5 pF

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5.3.6.5. Simulation of Actual Filter Frequency Response

An ideal frequency response is not possible in practice because it is necessary to use inductors and capacitors that not only possess finite Qs but also internal self-resonances due to parasitic elements. These factors, as well as parasitic effects due to board layout, may cause the actual frequency response to be degraded relative to the ideal response shown in Figure 29.

The effects of using non-ideal components can be predicted by simulation with SPICE models obtained from the manufacturers of discrete components, such as Murata or CoilCraft. Figure 31 shows the simulated frequency response of this low-pass filter design implemented with the real (i.e. lossy) 5% components given above. Although the filter attenuation at the second harmonic frequency (1732 MHz) is very strong (58.8 dB) and far exceeds the design goal of 28 dB minimum, the attenuation at 868 MHz is also very high (~2.59 dB). The introduced losses and parasitics deteriorate the filter response significantly and increase the useful band attenuation to an unacceptable level.

S21[dB] Non-Ideal 5th order Chebyshev response with 20% passband reflection and 908.6M cuttoff
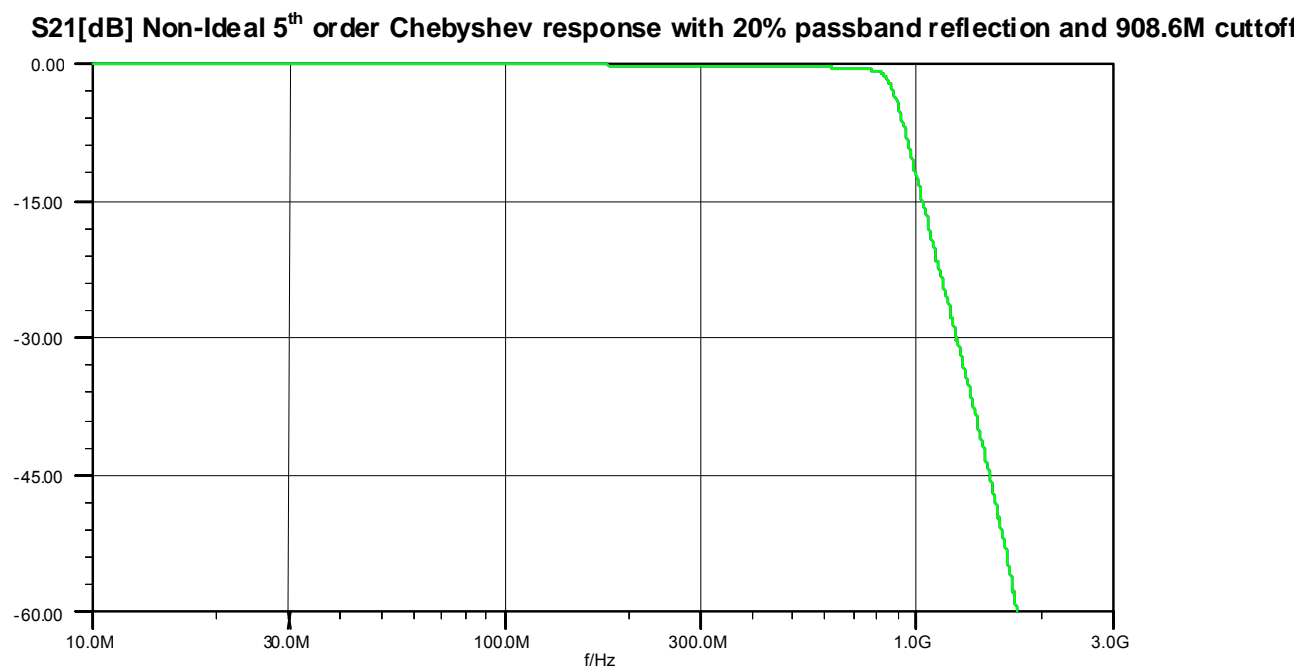
**Figure 31. Non-Ideal Simulated Freq Response of 0.17 dB Chebyshev Filter
(Fo = 868 MHz) with 5% Elements**

A possible solution is to tweak the filter first in the simulator and later on the bench. Basically, some harmonic attenuation can be sacrificed to get lower attenuation at 868 MHz. The new set of element values after tweaking are:

- CM = 2.7 pF
- LM = 9.1 nH
- CM2 = 5.1 pF

The non-ideal filter response after adjustment is given in Figure 32. Here, the cutoff frequency is shifted up; thus, the simulated attenuation at 868 MHz is approximately 0.32 dB. The second harmonic (1732 MHz) attenuation is still ~29 dB (1 dB better than the targeted 28 dB). In addition, due to the parasitics, the attenuation decreases at very high frequencies (10th harmonic and above), but is still around –40 dB, which is far enough for the low-level high harmonics. The filter attenuation at higher harmonics easily exceeds the design target of 28 dB, thus validating the choice of filter type, order, and passband amplitude ripple.

S21[dB] Non-Ideal 5th order Chebyshev response with 20% passband reflection after tweaking
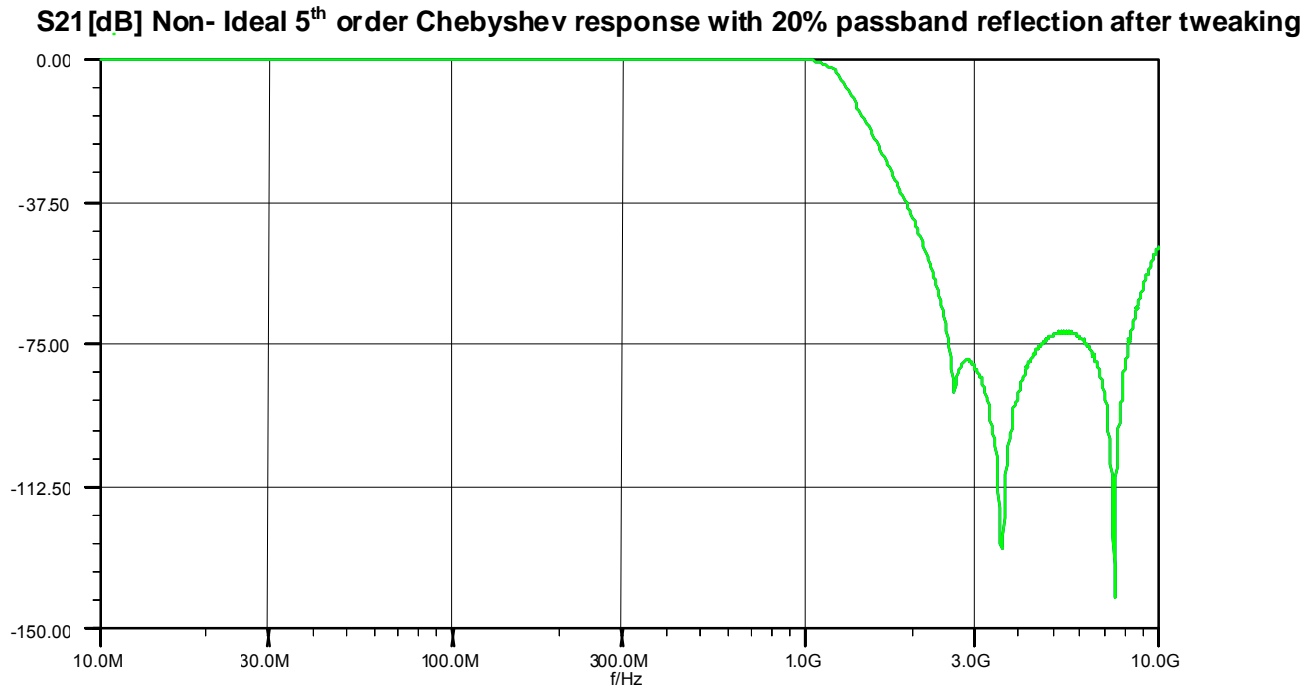
Figure 32. Non-Ideal Simulated Freq Response of 0.17 dB Chebyshev Filter after Adjustment (Fo = 868 MHz)

However, it should be clearly understood that Silicon Labs does not guarantee that a fifth-order low-pass filter design is appropriate for all customer applications. Depending upon the applicable regulatory standard and desired output power level, the filter order may need to be modified to suit a particular customer's needs.

It is apparent that there are transmission zeros in the simulated frequency response. These transmission zeros (e.g. near 3.6 and 7.45 GHz in Figure 32) are due to self-resonances in the discrete components. The shunt capacitors in the filter network (CM and CM2) exhibit a series self-resonance at some frequency, while the series inductors (L0, LM, and LM2) exhibit a parallel self-resonance at some frequency. The presence of such transmission zeros may help to "bend down" the attenuation curve more quickly, resulting in improved attenuation at lower harmonic frequencies, but at the cost of degraded attenuation at higher harmonic frequencies. Despite this, due to spreading issues, it is not advisable to rely too heavily upon "tuning" of these transmission zeros to aid in meeting harmonic performance.

5.3.6.6. Combining the LPF with the Output Match

The methodology used to design the low-pass filter was for a filter with a 1:1 impedance transformation ratio. That is, if the antenna impedance was R_{ANT} = 50 Ω, then the impedance seen looking into the input of the low-pass filter at C_M is also 50 Ω (at the fundamental frequency). Thus, our calculations for impedance matching components L_X and C_X remain unchanged. The resulting schematic for the output match and low-pass filter is shown in Figure 33.
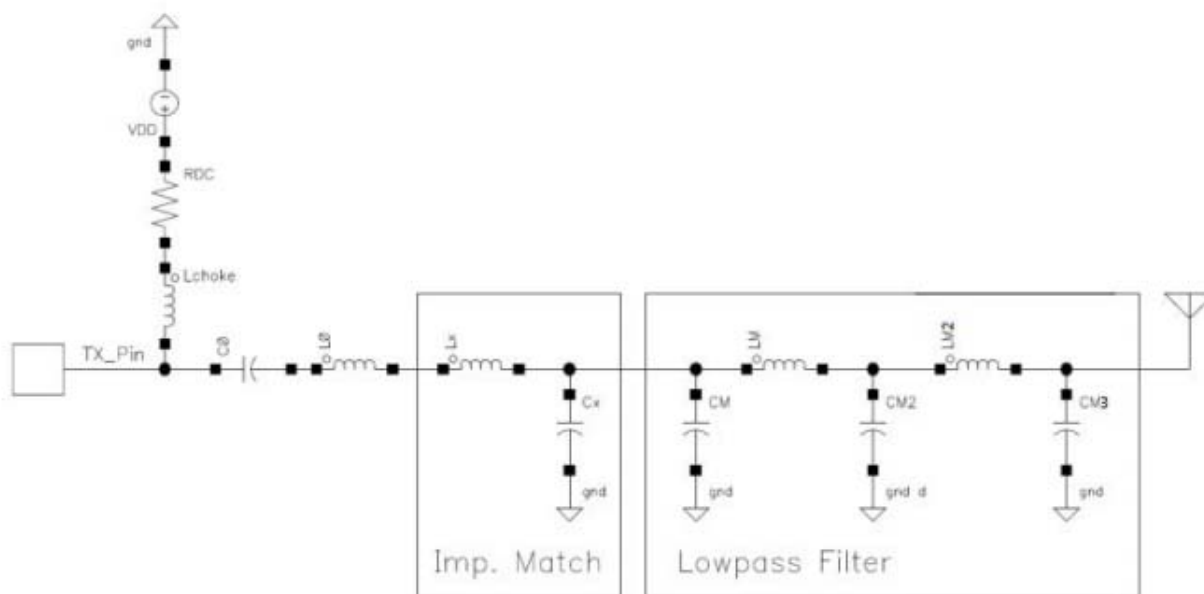
Figure 33. Schematic of Output Match and Lowpass Filter

However, it is quickly apparent that this schematic may be simplified. As discussed previously, series inductors L_0 and L_X may be combined into one equivalent series inductance. Shunt capacitors C_X and C_M may be combined in a similar fashion. After simplification, the schematic appears as shown in Figure 34. The combined value of L0 + Lx = 19 nH, while the combined value of CM + Cx = 6 pF.
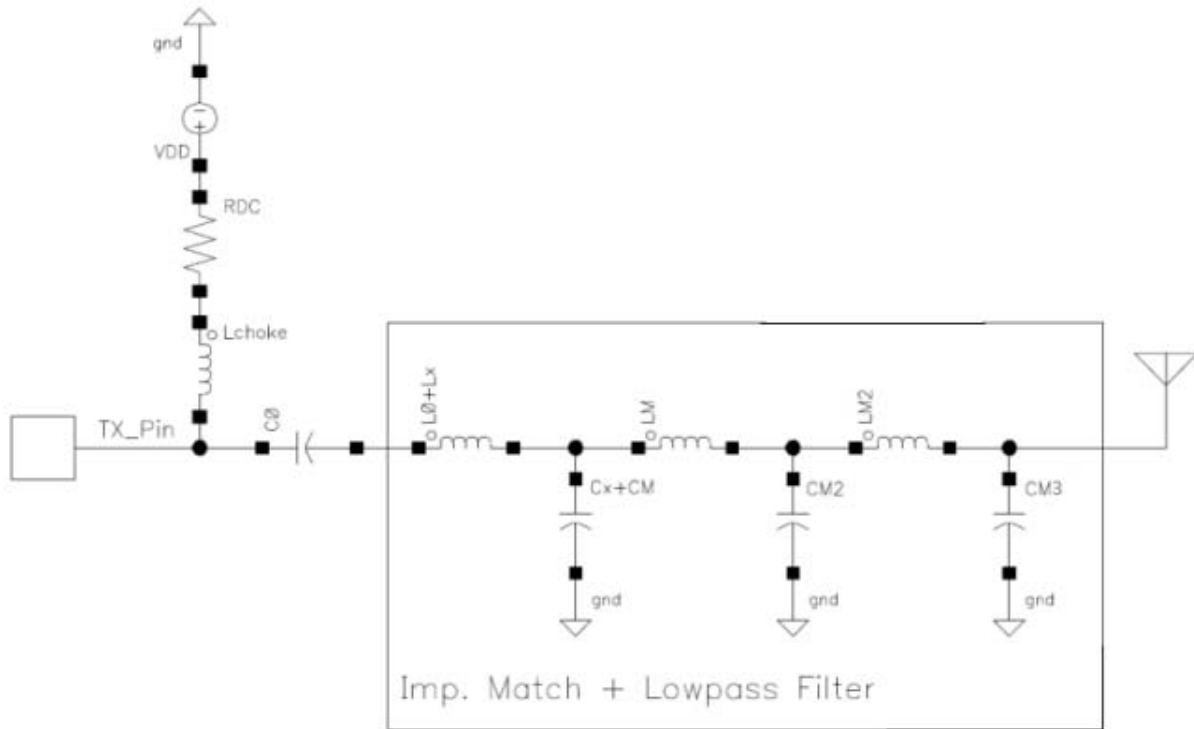
Figure 34. Schematic of Output Match and Lowpass Filter (Simplified)

After the filtered class E Tx match is finalized, some bench tuning is also advisable. As mentioned earlier, during the adjustment process, it was seen that the efficiency can be improved slightly if the shunt (CM + Cx, which, in any case, is denoted simply by CM in the tables in "2. Summary of Matching Network Component Values" on page 6) capacitor is reduced to 2.7 pF. Again, this sacrifices some second harmonic attenuation, but the harmonic spectrum still complies with a large margin (see Figure 35).

The final class E Split TX match component values are given for the Si4461 in Table 8 on page 13 and for the Si4060/Si4460/67 Table 15 on page 18.

5.3.6.7. Final Measurement of Harmonic Spectrum of the 13 dBm Class E High-Efficiency Match

The conducted output power spectrum of the final circuit is shown in Figure 35. These results are measured at the TX output power level setting of 0x31 of the Si4060/Si4460/67 RFIC with 22.8 mA total current consumption at 3.2 V supply voltage. As can be seen, the output power is approximately 0.5 dB lower than that without a filter, i.e the real lossy filter attenuation is approximately 0.5 dB. However, due to the reduced CM, the efficiency improved, and the total IC current is only 22.8 mA.
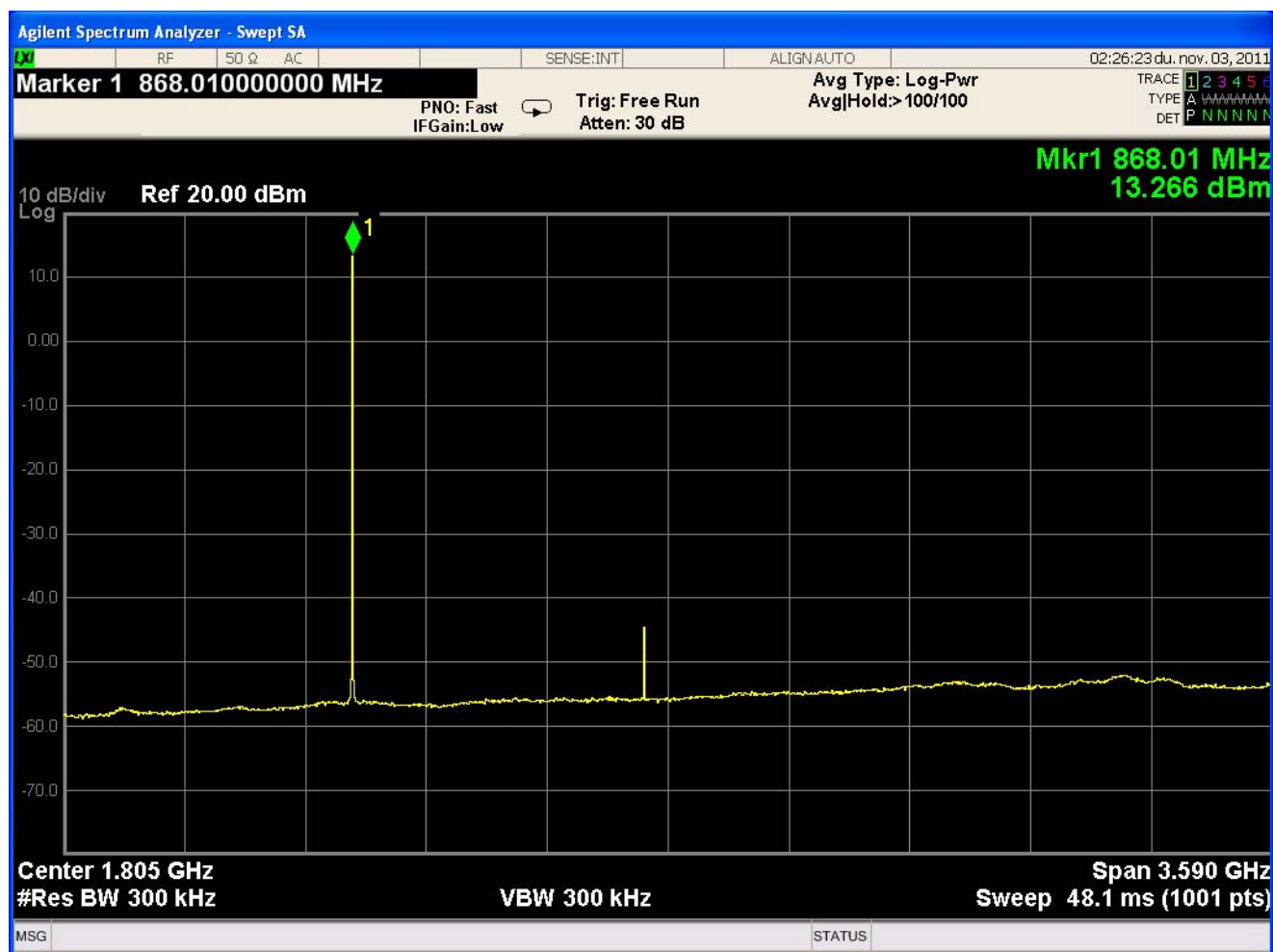
Figure 35. Filtered Harmonic Spectrum at Power State 0x31 (with 22.8 mA Total IC Current) of the 13 dBm Si4060/Si4460/67 High-Efficiency Class E Match (Fo = 868 MHz—See Table 14 on page 17)

5.3.6.8. Final Measurement of Harmonic Spectrum of the 10 dBm Class E Match

In theory, the 10 dBm Class E design should be the same as the 13 dBm one; only the power level is reduced properly by a lower power level setting. However, during bench tweaking, it is seen that the efficiency at low power levels can be improved further if the C0 value is increased slightly. The conducted output power spectrum of the final 10 dBm circuit (given in Table 14 on page 17) is shown in Figure 36. These results are measured at the TX output power level setting of 0x19 of the Si4060/Si4460/67 RFIC with 16.4 mA total current consumption at 3.2 V supply voltage.
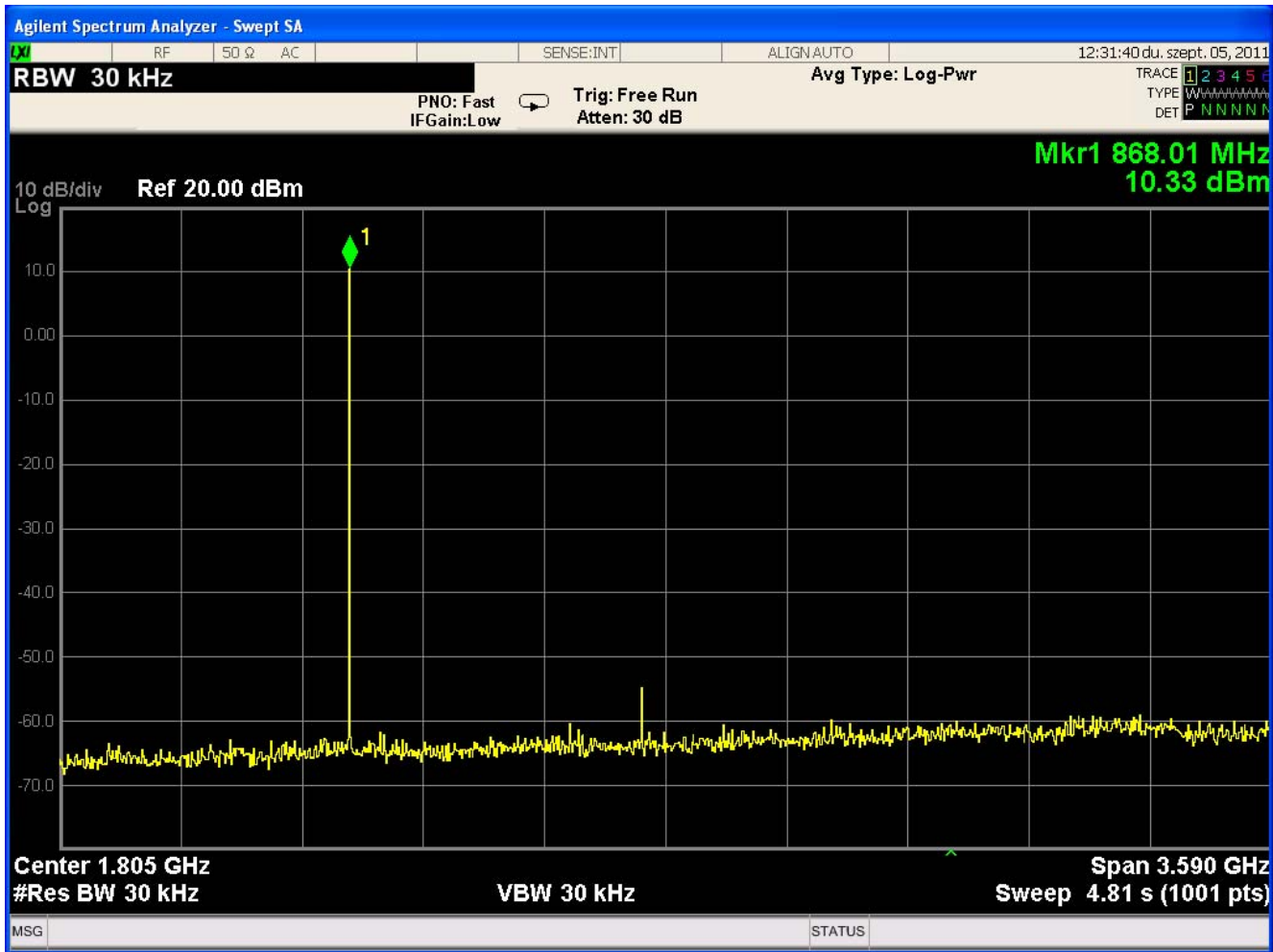
Figure 36. Filtered Harmonic Spectrum at Power State 19h of the Tuned 10 dBm Si4060/Si4460/67 Class E Match (Fo = 868 MHz—See Table 14 on page 17 for Component Values)

5.3.7. Summary of Match

This completes the steps of the match design process for the Split TX/RX board configuration. This match design process may be used to obtain matching component values at any desired operating frequency as well as for the Si4461. A summary table of these matching component values is shown in Tables 7 and 14.

5.4. Detailed Matching Procedure for Direct Tie Board Configuration

In the Direct Tie board configuration, the TX and RX paths are tied directly together without the use of an RF switch, as shown in Figure 37. Careful design procedure must be followed to ensure that the RX input circuitry does not load down the TX output path while in TX mode and that the TX output circuitry does not degrade receive performance while in RX mode.

The RX input circuitry of the EZRadioPRO 2 family of chips contains a set of switches that aids in isolation of the RX pins in TX mode. This set of switches is implemented internally as shown in Figure 37.
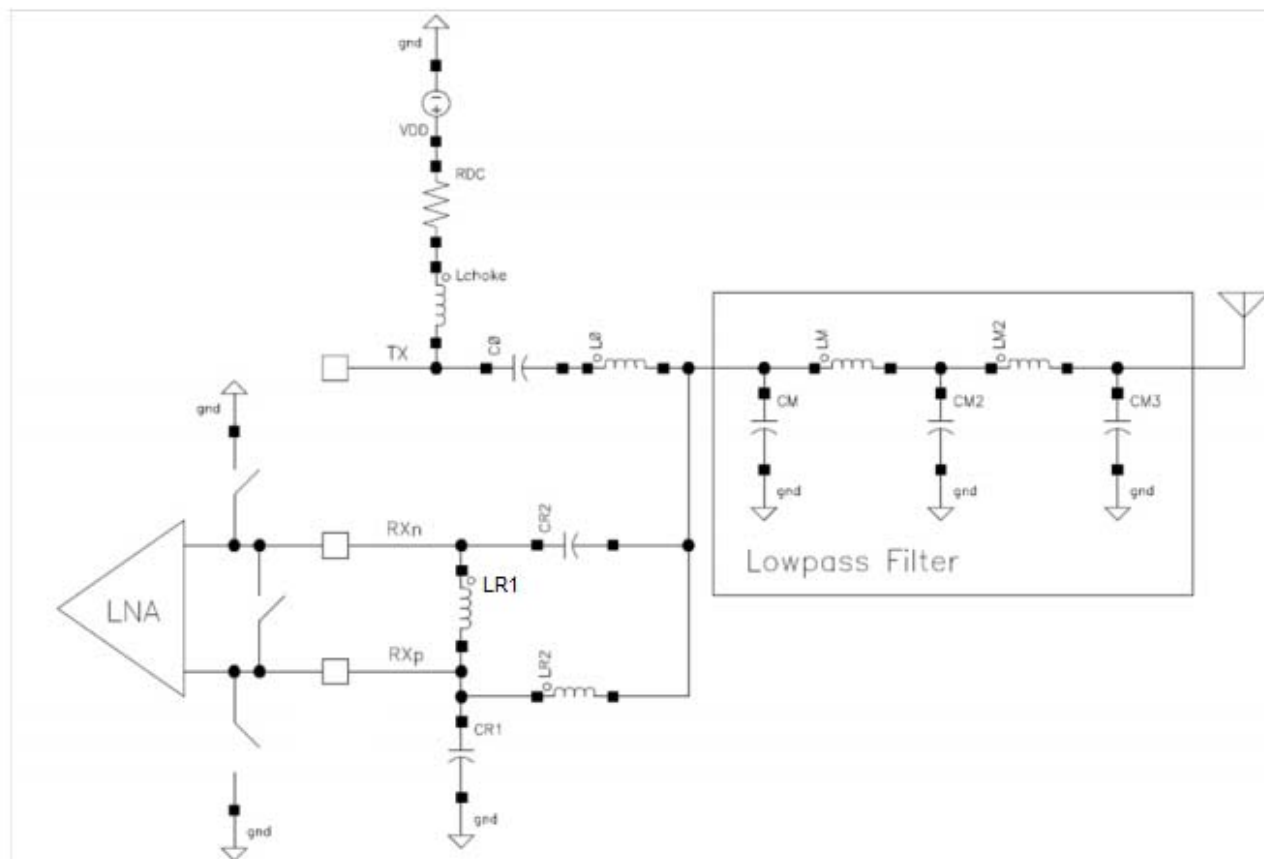
Figure 37. RX Input Switches for Direct Tie Operation

These three switches are activated simultaneously upon entering TX mode. They are opened only in RX mode and closed during all other modes (including TX mode).

Here, the operation in TX mode (when the switchers are closed) is the same as what was described in the case of the SWC DT match (see "3.2.1. Concept of Direct Tie Matching" on page 43); closing these switches during TX mode effectively shorts the RXp and RXn input pins together and shorts them to GND. The effective circuit may be redrawn as shown in Figure 38. Note that inductor LR2 and capacitor CR2 have been placed in parallel by the closure of the switches, and they are connected to GND. If the values of these components are chosen for resonance at the desired operating frequency, a very high impedance is presented to the TX path, resulting in very little degradation in TX output power. Also, by shorting the input pins of the LNA together and simultaneously to GND, the LNA is protected from the large signal swing of the TX signal. This feature allows connection of the TX path to the RX path without damage to the LNA.
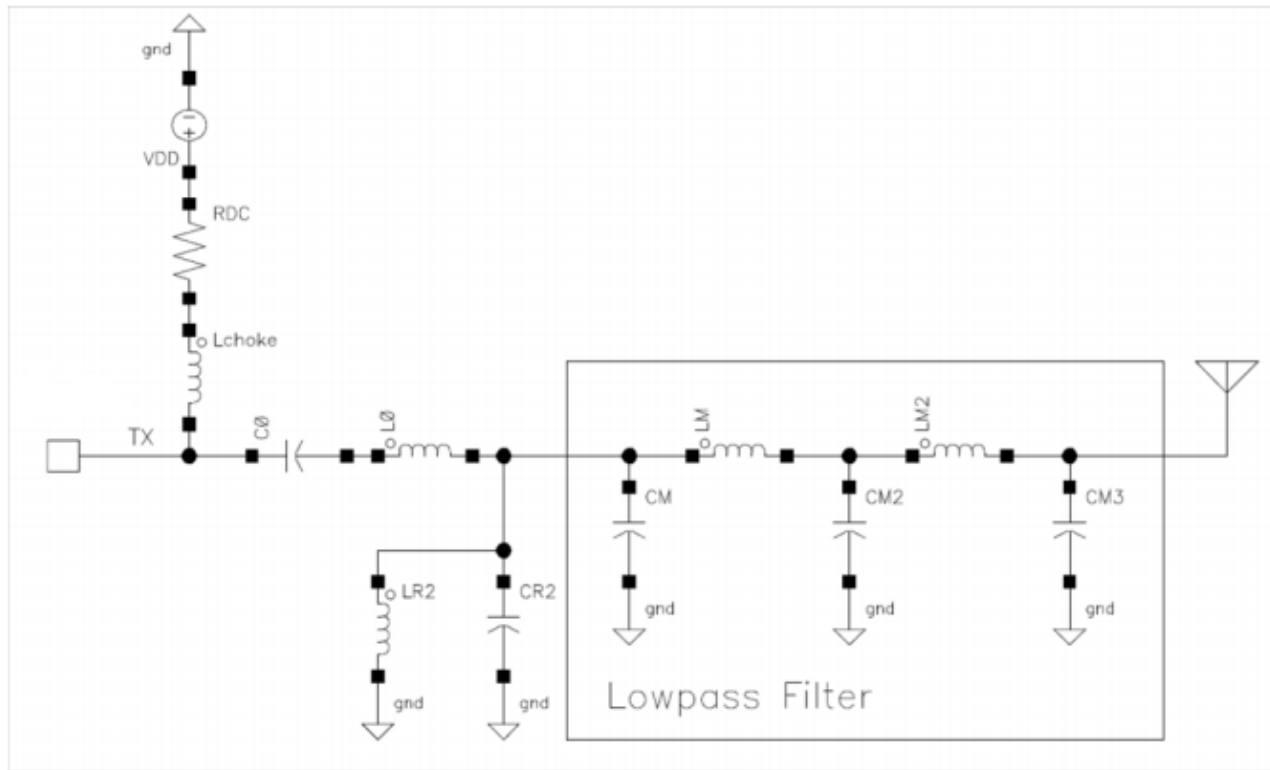
Figure 38. Effective Direct Tie Circuit in TX Mode

In RX mode, the output transistors of the PA are in the OFF state, and the impedance seen looking back into the TX pin is comprised mostly of the output capacitance of the transistors. (The impedance of the pull-up inductor, L_{CHOKE}, is quite high and may be ignored for this discussion.) This OFF stated PA output capacitance value, C_{PAOFF}, is not much different from the ON STATED value. In the case of a Class E match, this PA capacitance is effectively in-series with matching capacitor C0 and results in series-resonance with inductor L0 at some frequency, as shown in Figure 39. At this series-resonant frequency, the input to the LNA matching network (LR2, CR2, LR, CR1) is effectively shorted to GND and thus significantly degrades receive performance. As the PA output capacitance, C_{PAOFF}, is fixed, it is necessary to choose L0 and C0 to ensure that this series-resonance does not excessively degrade RX performance at the desired operating frequency. It may be necessary to alter the values of L0 (variation of C0 is less efficient as it is in-series with the fixed C_{PAOFF}) slightly away from their calculated optimum values in order to accomplish this goal, thus slightly degrading TX performance in an effort to minimize the impact to RX performance.

With the typical C_{PAOFF} values of the Si4460/61/67 RFIC family, this effect is most critical at the upper frequency bands (868 or 915 MHz). At lower frequency bands (169 or 434 MHz) it usually does not cause any problems, and the DT TX match element values are identical to the values of the Split TX/RX configuration.
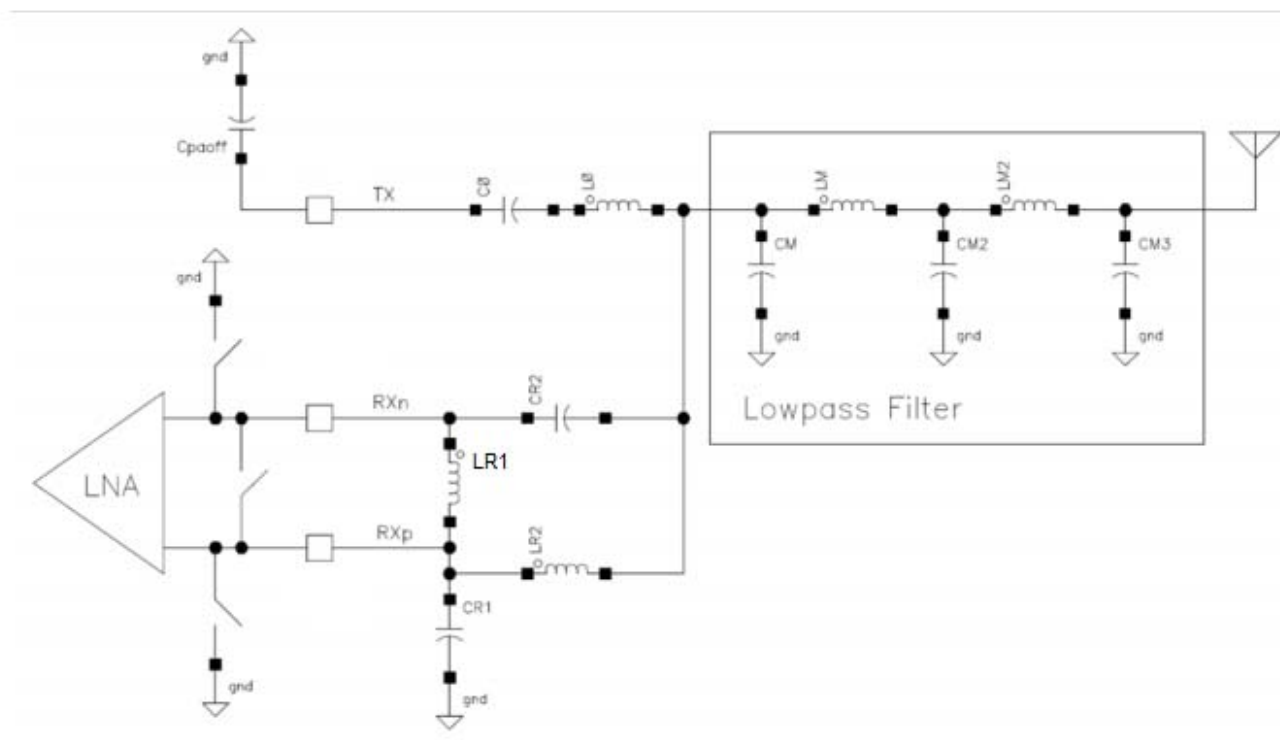
Figure 39. Effective Direct Tie Circuit in RX Mode

We next provide further detail about each step of the matching procedure for the Single Antenna with Direct Tie board configuration. Again, assume a general chip supply voltage of V_{DD_RF} = 3.3 V. Our design example will be constructed for Si4460/67 for the 868 MHz ETSI band, with a targeted output power level of +13 dBm.

5.4.1. Steps #1–6: Same Design Procedure as for Split TX/RX Board Configuration

Steps 1 through 6 are exactly the same as those shown in "5.3. Detailed Matching Procedure for Split TX/RX Board Configuration" on page 60.

5.4.2. Step #7: Design RX Input Match

In Step #7, we design an impedance matching network for the differential RX input. The RX matching network is comprised of a total of four inductors and capacitors (LR2, CR2, LR, CR). The goals for this network are as follows:

- Match the LNA input to a 50 Ω source impedance (i.e., the antenna)
- Provide a single-ended to differential conversion function (i.e., a balun)
- Ensure that LR2,CR2 are parallel-resonant at the desired operating frequency

The design equations (and their mathematical derivation) for selection of the matching component values are discussed in detail in "AN643: Si446x/Si4362 RX LNA Matching". This procedure is also the same one described in "3.2.4. Construction of RX Match" on page 47. The following equations are introduced here without proof or further discussion; refer to AN643 for further details.

$$L_{R2} = \frac{\sqrt{50\ \Omega \times R_{LNA}}}{\omega_{RF}}$$

Equation 30.

$$C_{R2} = \frac{1}{\omega_{RF}^2 \times L_{R2}}$$

Equation 31.

$$C_{R1} = 2 \times C_{R2}$$

Equation 32.

$$L_{LNA} = \frac{1}{\omega_{RF}^2 \times C_{LNA}}$$

Equation 33.

$$L_M = 2 \times L_{R2}$$

Equation 34.

$$L_{R1} = \frac{L_{LNA} \times L_M}{L_{LNA} + L_M}$$

Equation 35.

Note that our goal of parallel-resonance between LR2 and CR2 is inherently satisfied, as evidenced by Equation 31.

At any given frequency, the differential input impedance at the RX pins of the chip may be represented by an equivalent parallel R-C circuit; their values are represented by the parameters R_{LNA} and C_{LNA} in the above equations. It is necessary to know these equivalent circuit values at the desired frequency of operation, prior to constructing the match.

The differential input impedance of the RX port on the Si446x RFIC is provided in AN643. The values of R_{LNA} and C_{LNA} at a desired operating frequency of 868 MHz are found to be R_{LNA} = 380 Ω and C_{LNA} = 1.09 pF. After plugging these values into the above equations, the following ideal matching component values are calculated:

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- LR2 = 25.27 nH
- CR2 = 1.33 pF
- LR1 = 19.15 nH
- CR1 = 2.66 pF

In practice, it is often necessary to slightly modify the matching component values suggested by the above equations. Any printed circuit board layout has parasitics, such as trace inductances or component pad capacitances, and these may have an effect upon the circuit. Silicon Labs has empirically determined that if 0402-size wire-wound or multilayer inductors are used on the Direct Tie reference board designs (available at www.silabs.com), the actual component values are as shown in the 868 MHz rows in Table 16 on page 19 for the wire-wound case and reproduced below:

- LR2 = 24 nH
- CR2 = 1 pF
- LR1 = 20 nH
- CR1 = 3 pF

The above inductor element values are not available in multilayer type; so, new bench-optimized multilayer RX match elements are necessary and are given in Table 18 on page 20.

Although not required, it is useful to measure the input impedance seen looking into the RX match in both RX mode as well as TX mode. Obviously, it is desired to verify a good match to 50 Ω while in RX mode in order to obtain optimum sensitivity. However, it is also useful to verify that the network provides a high impedance while in TX mode (when the switches at the input of the LNA (see Figure 38) are in their CLOSED position, and thus LR2 and CR2 form a high-impedance parallel-resonant network, which isolates the RX path from the TX path); otherwise, the RX circuitry may excessively load down the TX path. Specifically, it may be necessary to slightly adjust the values of LR2 and/or CR2 to achieve optimum parallel resonance at the desired frequency of operation.

The isolation in TX mode is more critical with multilayer inductors since this type has lower Q (higher loss), and the values are available in rarer steps. So both to achieve high impedance at LR2-CR2 parallel resonance and also to tune the resonance exactly to the frequency of operation is more difficult.

The actual measured impedance of the 868M multilayer RX match while in TX mode is shown in Figure 40 and confirms the expectations of "good enough" isolation; the measured impedance at 868 MHz is ~452 Ω + j593Ω, which corresponds to a parallel R-C equivalent of 1.2 kΩ – 0.196 pF. This slight parallel capacitance (~196 fF) may be ignored.
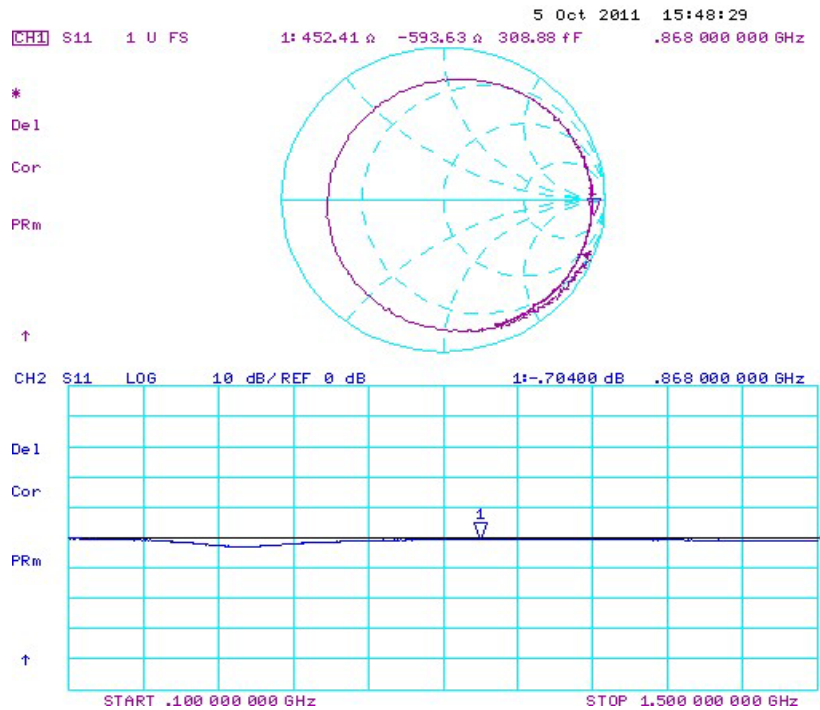
Figure 40. RX Match Input Impedance in TX Mode, Multilayer 868M Type

The measured impedance at the input of the multilayer RX matching network while in RX mode is shown in Figure 41. It is observed that the input impedance is quite close to 50 Ω, with the network providing S_{11} with better than 15 dB return loss.
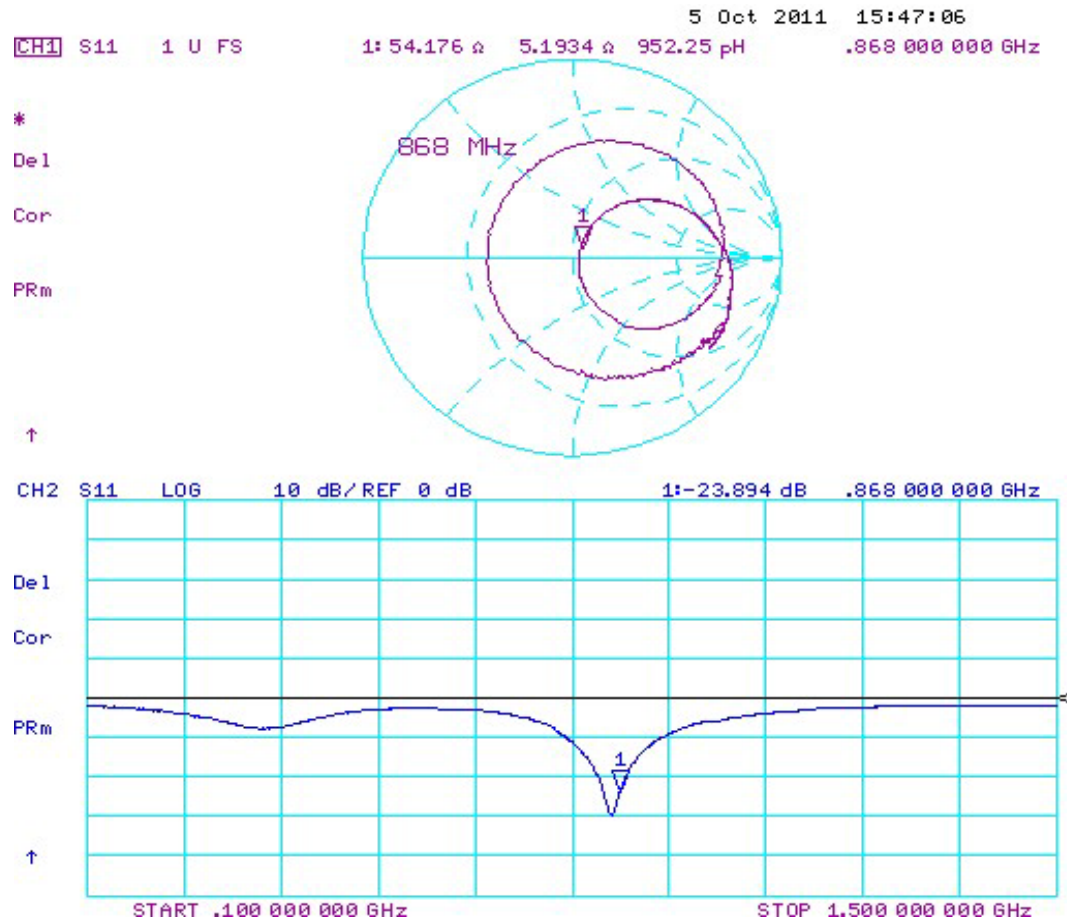
Figure 41. RX Match Input Impedance in RX Mode, Multilayer 868M Type

5.4.3. Step #8: Slightly Modify the Value of L0

In Step #8, we deliberately mistune the value of matching inductor L0 slightly away from its optimum value, as determined in Steps 1 through 6. As illustrated in Figure 39 on page 81, the series-resonance of L0-C0-C_{PAOFF} has the potential to significantly degrade the RX performance by placing a (near) short to GND at the input of the RX matching network. It is important that this series-resonant frequency be adjusted to fall sufficiently far away from the desired operating frequency in order to minimize its effect upon RX sensitivity.

This is accomplished by deliberately increasing or decreasing the value of L0. Here, the variation of C0 is not efficient as it is in series with the fixed C_{PAOFF}; thus, higher deviation from the optimum class-E value would be necessary to achieve the same detuning.

In the 868/915 MHz band and in RX mode, the Si4461 usually needs to have L0 increased (compared to the split TX/RX case) in order to shift away the L0-C0-CPAOFF parasitic resonance while, for the Si4460/67, the L0 usually needs to be decreased in order to shift away the L0-C0-CPAOFF parasitic resonance.

This will push the unwanted resonance lower or higher in frequency and minimize its effect upon RX performance. A typical aim is to suffer less than 2 dB sensitivity degradation at direct tie mode compared to the split TX/RX case.

Some post-tuning of capacitor CM may also be required to improve Class-E operation in TX mode after the change in value of L0.

The value of PA output capacitance in its OFF state may be slightly different than the value of shunt drain capacitance C_{SHUNT} (discussed in "5.3.3. Step #3: Calculate the Required Value for ZLOAD" on page 61). The value of C_{PAOFF} may be measured with a network analyzer connected to the TX output pin with all matching components removed, except for those providing dc bias (i.e., L_{CHOKE} and R_{DC}). Silicon Labs has performed this measurement and determined the value of C_{PAOFF} to be ~1.5 pF in the frequency range of 868 MHz to 950 MHz and 1.4 pF at low bands (315/434M). This is shown by the impedance measurement of Figure 42. The value of L_{CHOKE} must be chosen appropriately to provide a very high impedance at the frequency of interest; otherwise, the measured value of C_{PAOFF} may be affected.
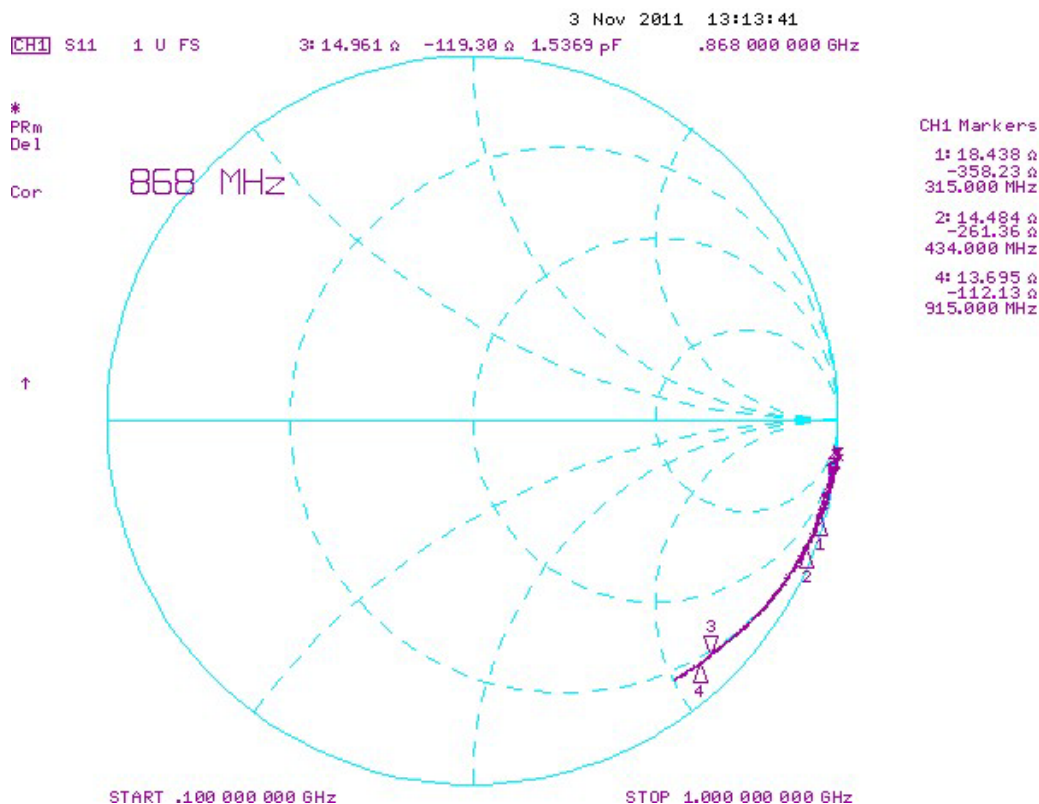
Figure 42. PA Output Capacitance Measurement of Si4460/67 in OFF State

Once the value of C_{PAOFF} has been determined, its effect upon RX performance may be estimated. Continuing with our design example at 868 MHz with the 13 dBm wire-wound split TX/RX board design, we find initial values of L0-C0 to be:

- L0 = 19 nH
- C0 = 3.6 pF

This value of capacitance of C0 is in series with C_{PAOFF} = 1.5 pF, resulting in an equivalent series capacitance of C_{EQUIV} = 1.06 pF. The series-resonant behavior of the resulting L-C circuit may be simulated and is shown in Figure 43; here, the S21 of the TX path is simulated from the filter outputs to the DT point with the L0-C0-C_{PAOFF} part. It can be observed that this L0-C0-C_{PAOFF} circuit introduces only ~0.8 dB of loss at 868 MHz, which is mostly the filter attenuation. Since this circuit is directly connected to the input of the RX match, this will result in approximately 0.8 dB of degradation in RX sensitivity, which is acceptable. It is also clear from the curve that the critical shunt of the RX path occurs far above 1 GHz.
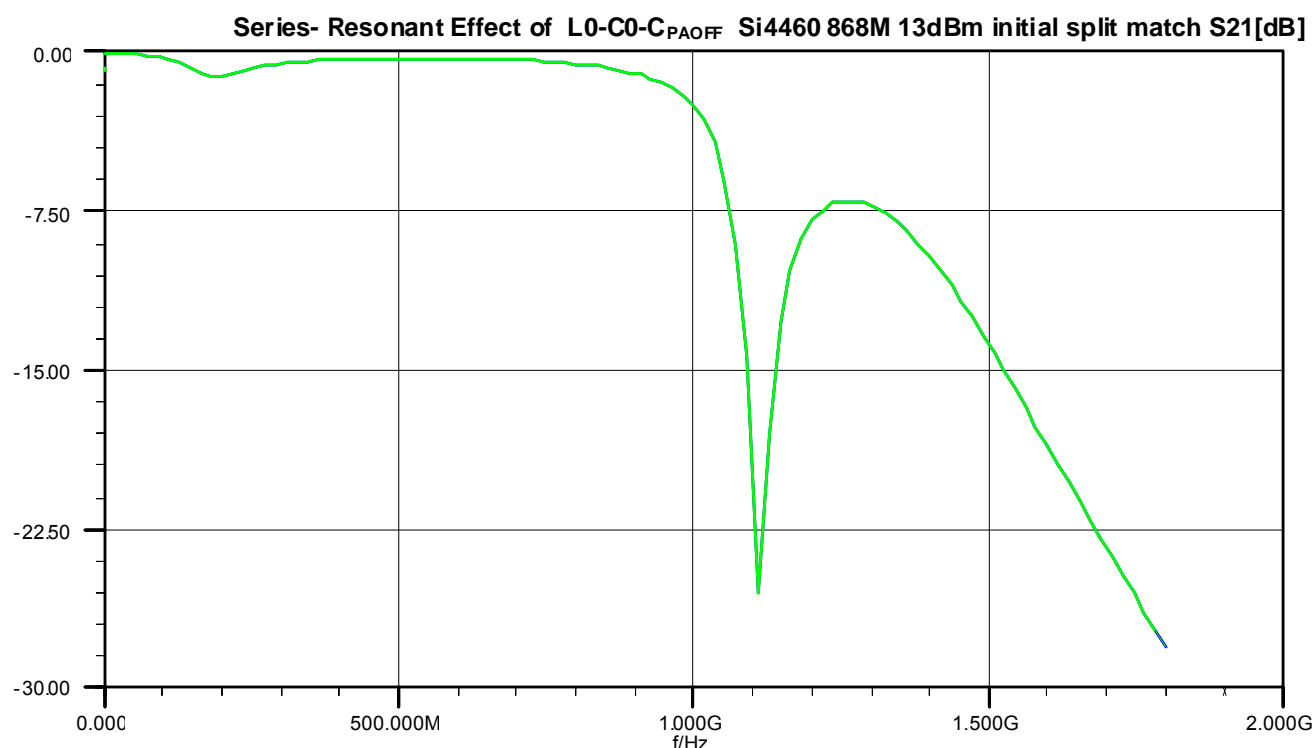
Figure 43. Series-Resonance Behavior of Initial L0-C0 Circuit of Si4460/67 13 dBm Split Class E Match

Unfortunately, the situation is more critical in case of the Si4460/67 10 dBm direct tie. There, the initial split C0 value is much higher (see Table 14 on page 17) in order to achieve better efficiency at reduced power levels. With the initial values of:

- L0 = 19 nH
- C0 = 15 pF

The parasitic L0-C0 – C_{PAOFF} series resonance curve is shown in Figure 44. As can be observed, due to the higher C0, the resultant C_{EQUIV} capacitance is 1.36 pF, and, thus, the resonance is at lower frequencies closer to the useful band. It results in an attenuation of ~2.5 dB according to the simulations. In real bench circumstances, the degradation in RX mode was even higher, approx 3.5 dB, which is unacceptable.

The resonant frequency of these circuit components may be shifted further upwards (away from the desired operating frequency) by decreasing the value of L0. Using our rule-of-thumb of decreasing L0 by ~20%, we arrive

at a modified value of L0 = 15 nH. In theory, with the 20% L0 variation, the class E operation in TX mode is still satisfactory, and, usually, the sensitivity degradation in RX mode will improve to be less than ~2 dB. However, in the case of the +10 dBm 868 MHz Si4460/67 DT match, the bench test of this modified circuit still did not show sufficiently good sensitivity in RX mode.

So, the L0 was decreased further to 12 nH with a parallel increase of C0 to keep the optimum class E TX operation. Simulation of the series-resonant behavior of the modified circuit is shown in Figure 45.

It is seen that the loss at 868 MHz has now been improved significantly to only ~0.9 dB in the simulations. In the bench test, the suffered RX sensitivity degradation is only ~1.1 dB, very close to the simulated value. While this still represents a 1.2 dB reduction in RX sensitivity, this is a good compromise between TX and RX performance.

Although this (12 nH and 27 pF pls. see Table 16 on page 19) set of L0-C0 values is proper for 868M 10 dBm operation, it is not good at 915M. Since dual band CLE TX operation seems to be feasible with minimum compromise, it makes sense to create a dual band DT circuit as well.

To have good Rx sensitivity at 915M the L0-C0-CPAOFF resonance has to be shifted up further. So, the new proposed L0 value is 6.8 nH and the new C0 values is 36 pF (Table 16) to have both moderate Rx sensitivity degradation at 915M and to maintain the acceptable TX class E operation at 868M and 915M.
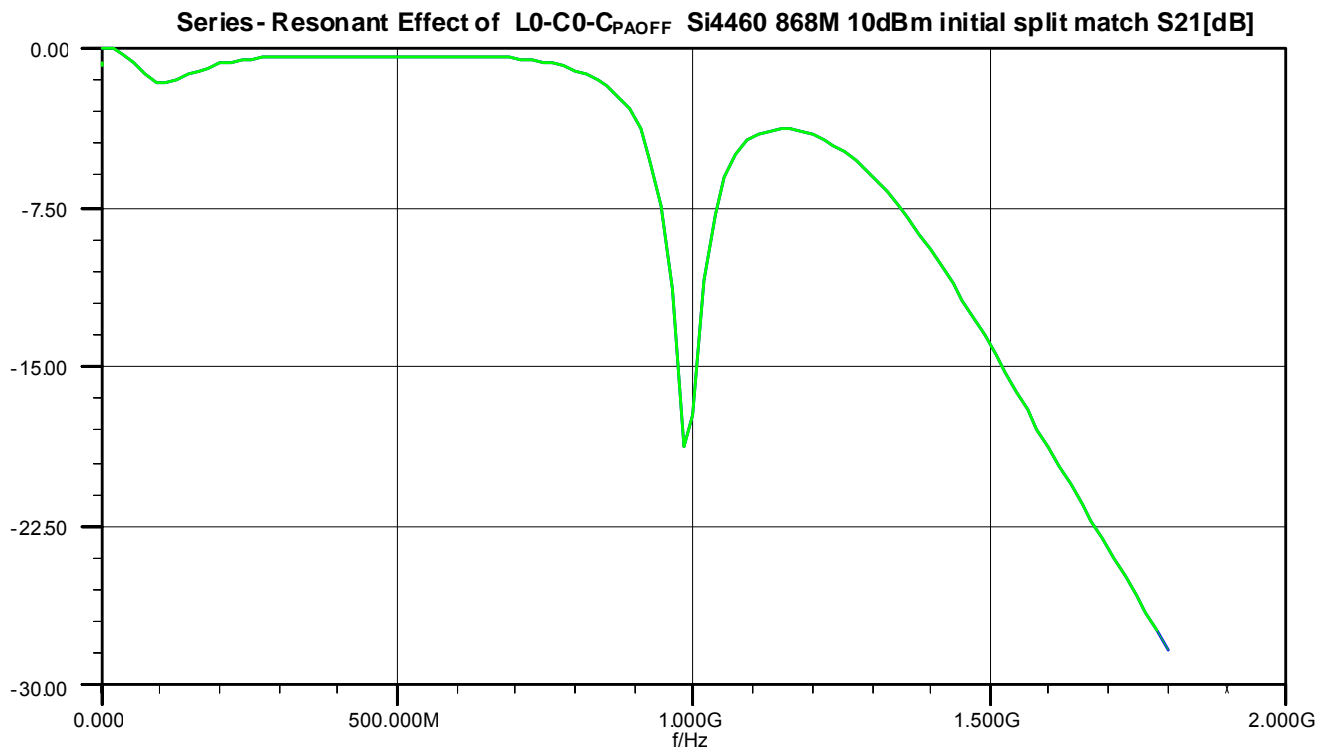
Figure 44. Series-Resonance Behavior of the Off-Stated Si4460/67 PA with the Initial 10 dBm 868M Split Class E L0-C0 Circuit (19 nH–15 pF)
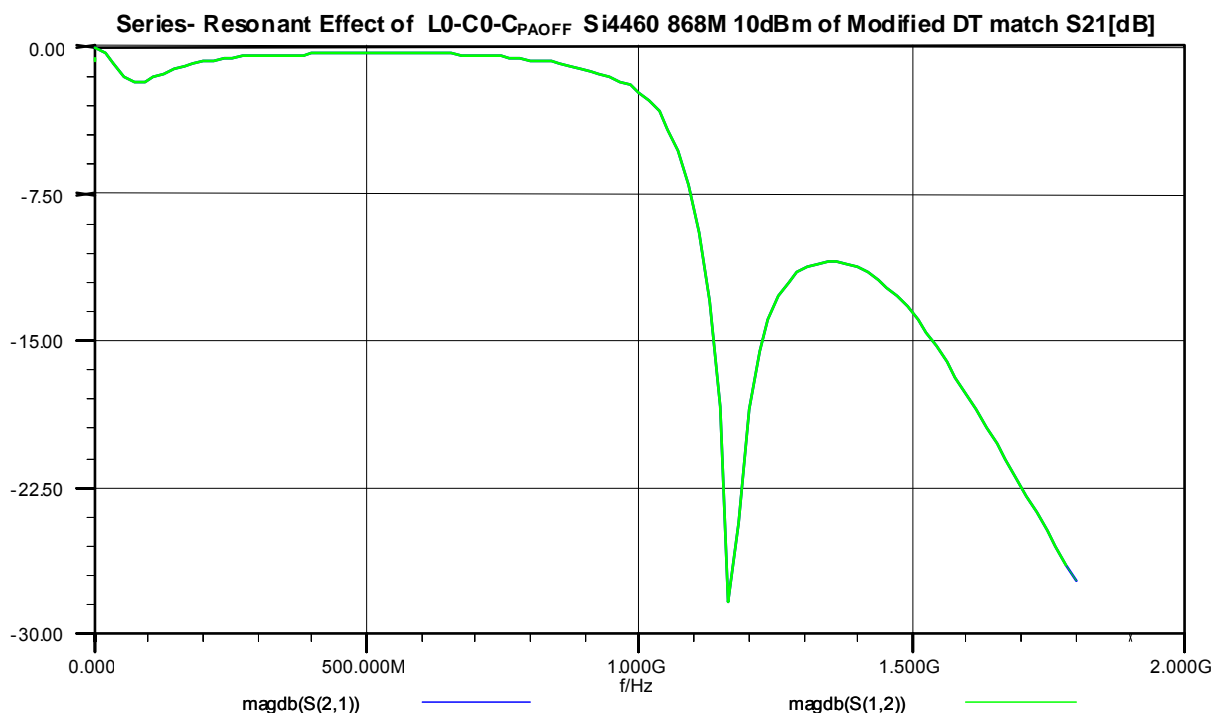
Figure 45. Series-Resonance Behavior of the Off-Stated Si4460/67 PA with the modified 868M 10 dBm Split Class E L0-C0 Circuit (12 nH–27 pF)

It is also possible to increase the resonant frequency of the L0-C0-C_{PAOFF} circuit by decreasing the value of C0 instead of L0. Here, it important to note that the increase of the C0 capacitor will have a reduced effect on the parasitic series-resonant frequency since the value of C_{PAOFF} is significantly lower than that of C0, and, thus, C_{PAOFF} determines primarily the resonance. Hence, a much larger increase of C0 is required to achieve the same resonance shift. This stronger mistuning will result in even greater reduction in performance in TX mode. Therefore, tuning of L0 is preferred and generally results in a better compromise between TX and RX performance.

This increase in the value of L0 is usually required only when working in the upper frequency bands, such as 868/915/950 MHz. In the lower frequency bands (315/390/434 MHz), the values of L0 and C0 obtained for the Split TX/RX board configuration usually continue to work well with the Direct Tie board configuration.

In the final circuit realization on Silicon Labs reference design boards, the value of capacitor CM was reduced to 1.5 pF to provide slightly better TX output power. The final Si4460/67 element values with wire-wound inductors are summarized in Table 16 on page 19. For Multilayer inductors, the same is given in Table 18 on page 20.

For the Si4461, the DT board element values are summarized in Tables 9, 11, and 14, both for wire-wound and multilayer inductor types.

Note that some small degradation in both TX and RX performance is expected for a Direct Tie configuration. That is, it is not possible to directly connect the TX and RX paths and achieve perfect isolation between the two circuit functions; each path will result in some amount of unwanted loading to the other path, and, thus, some there will be slight degradation in performance (relative to a Split TX/RX board configuration in which the TX and RX paths remain entirely separate). The choice of matching inductor L0 heavily impacts the trade-off between optimizing for TX output power at the expense of degraded RX sensitivity, or vice-versa. A value may generally be found that achieves a good compromise between the two, typically resulting in less than 1 dB reduction in TX output power and no more than 2–3 dB reduction in RX sensitivity. Some amount of "tweaking" of the final values of L0 and CM may be necessary to achieve the best compromise.

5.4.4. Summary of Match

This completes the steps of the match design process for the Direct Tie board configuration. This match design process may be used to obtain matching component values at any desired operating frequency.

APPENDIX A—MEASURED SPECTRUM PLOTS

The following section presents some measured spectral data plots on different CLE board configurations in TX mode at a variety of frequencies given in "2. Summary of Matching Network Component Values" on page 6. Measured results for circuit realizations with both wire-wound inductors and multi-layer inductors are presented.

Si4461 Measured Plots

Si4461 Split TX/RX Board CLE Configurations with Wire-Wound Inductors
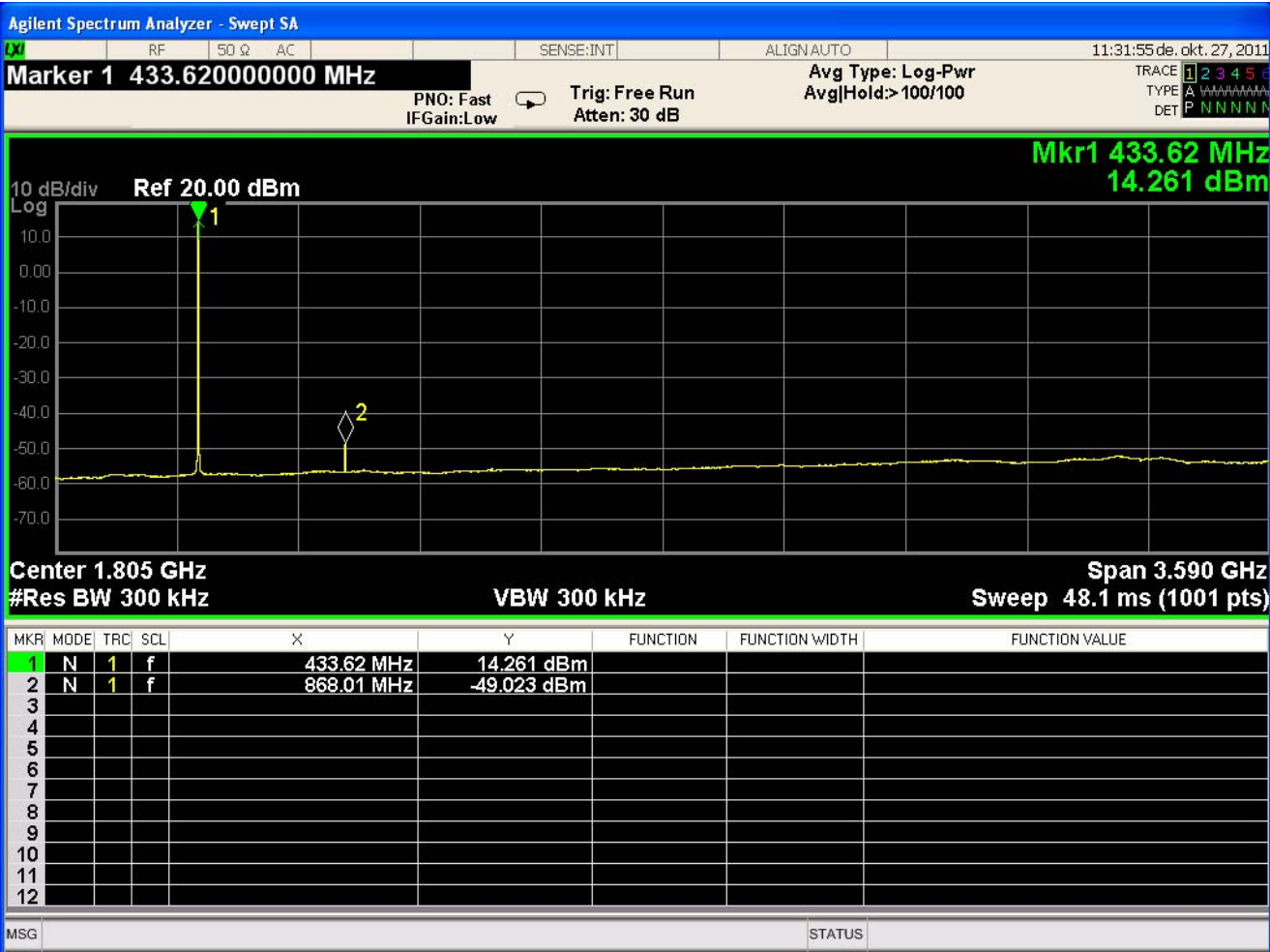
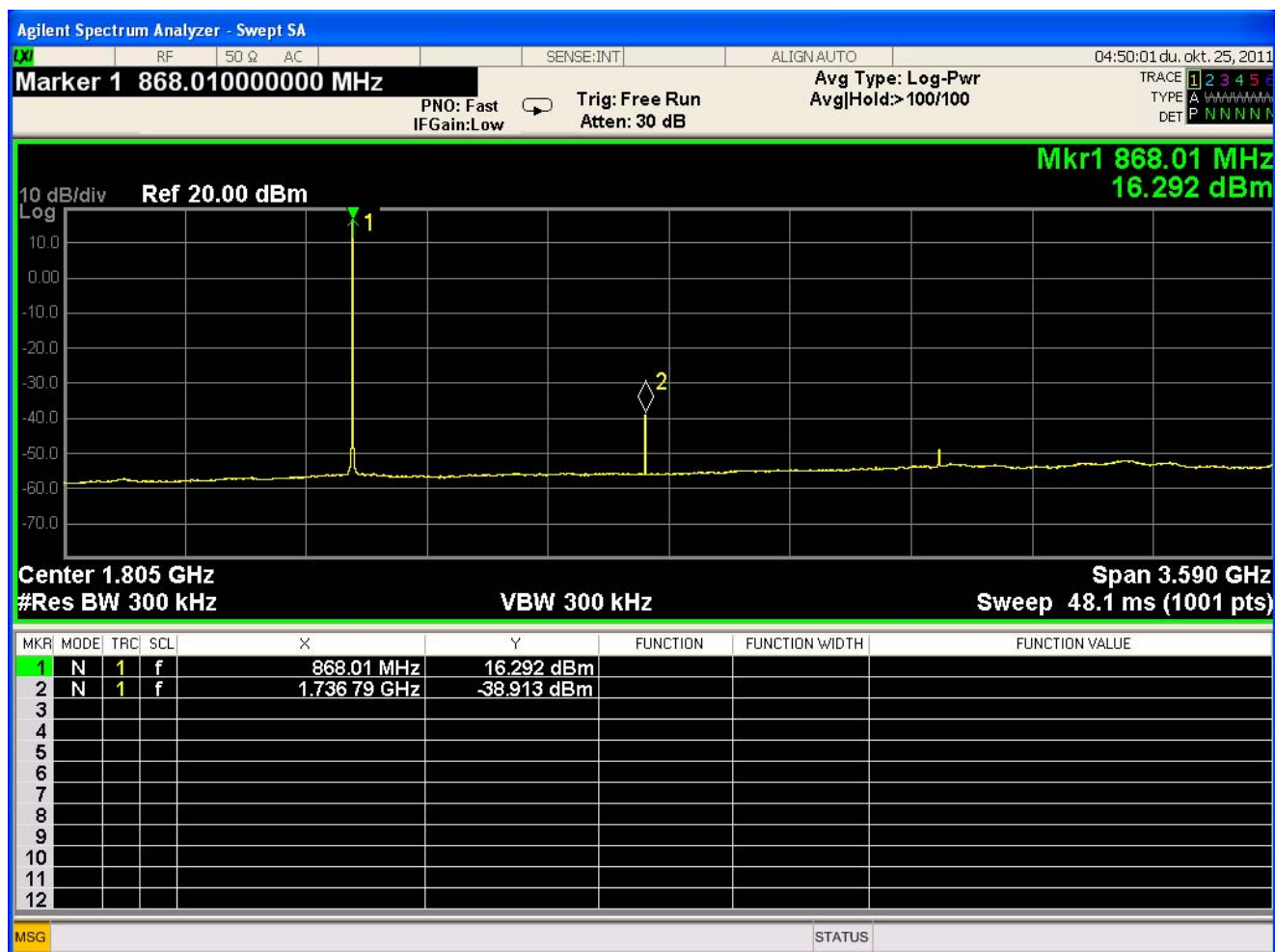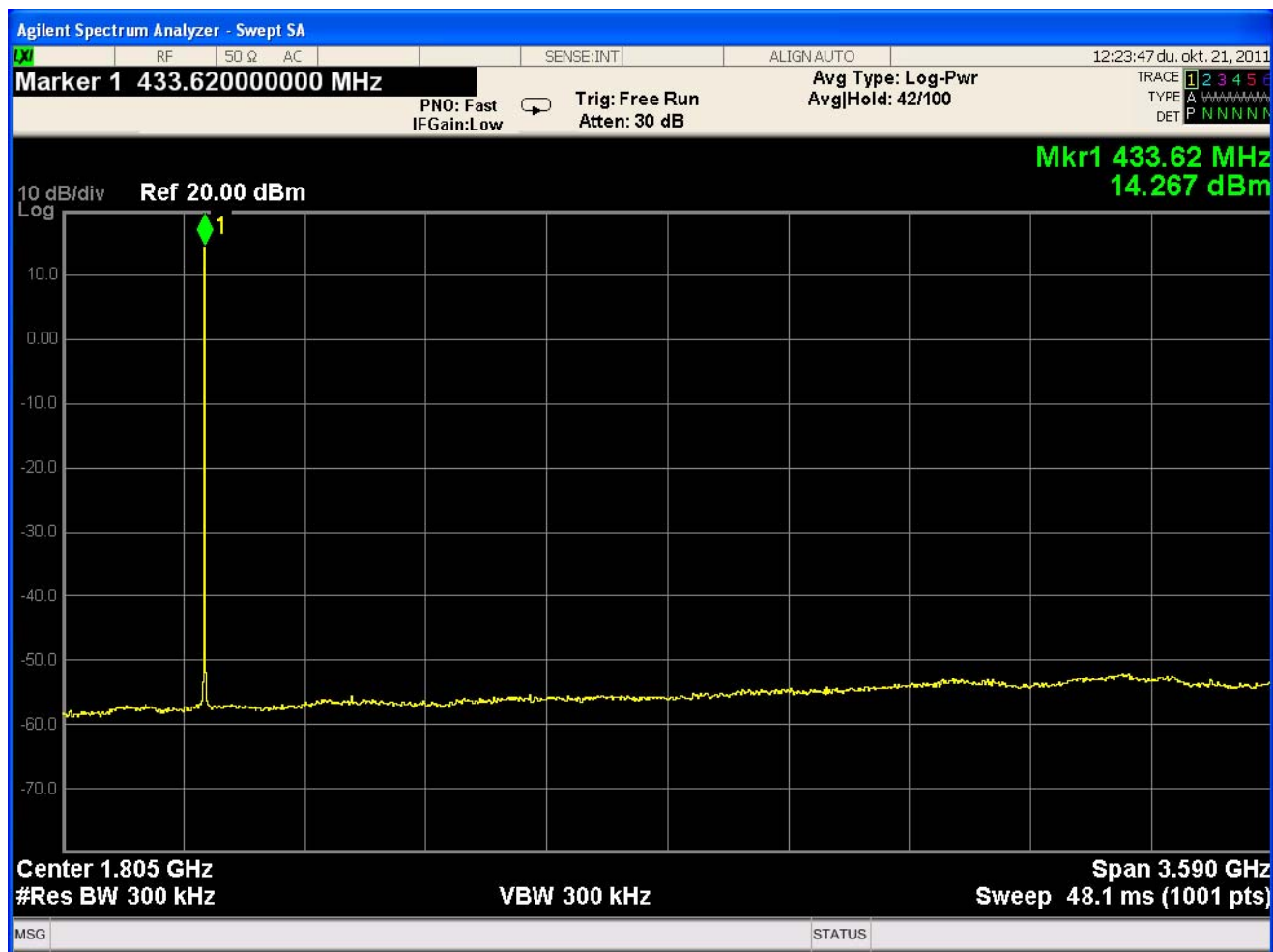**Figure 46. Si4461 14 dBm Split TX/RX Board at 434 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x20, 28.1 mA**
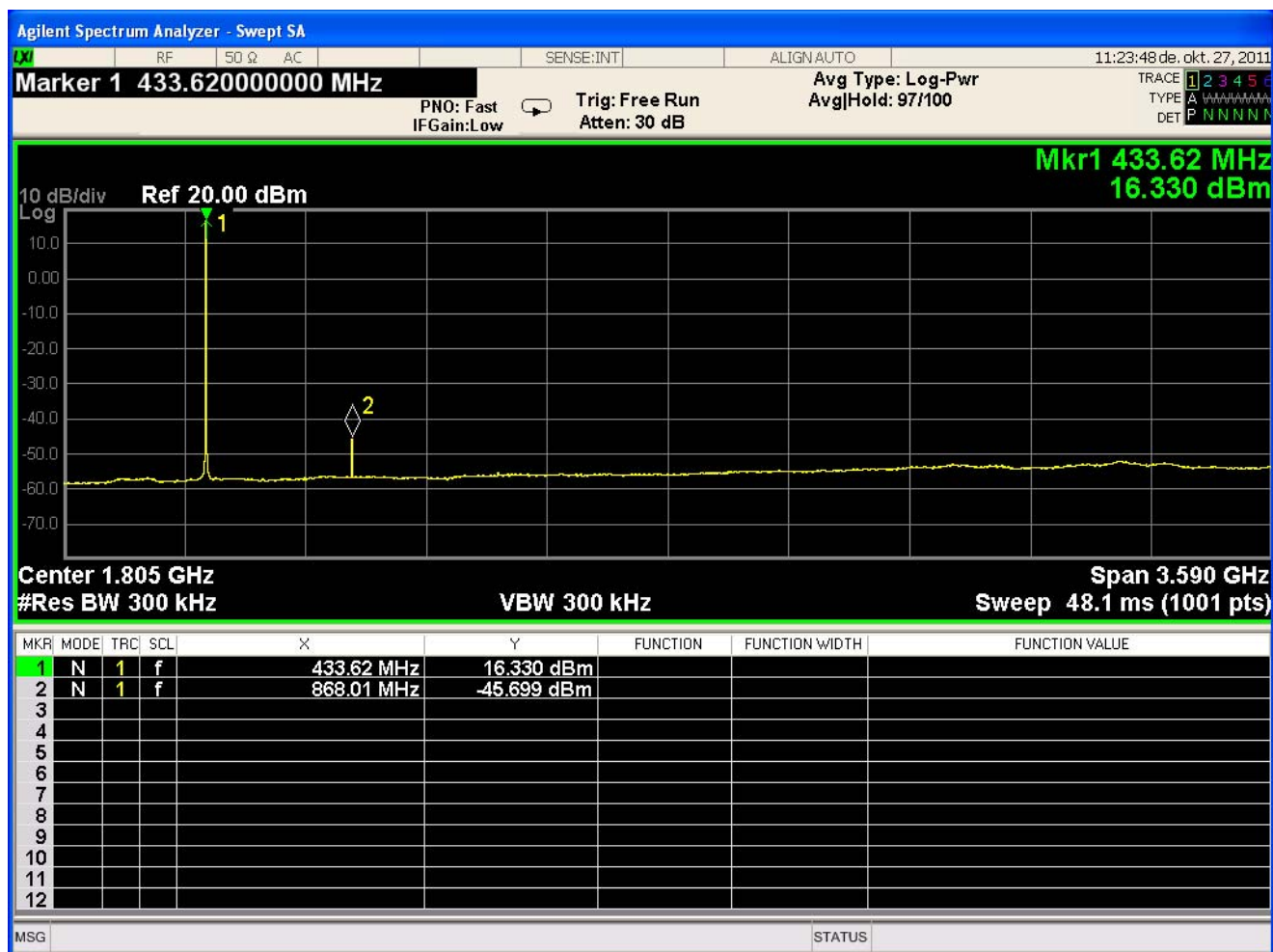
Figure 47. Si4461 16 dBm Split TX/RX Board at 434 MHz with Wire-Wound Inductors, V$_{DD}$ = 3.2 V, DDAC[6:0] field in the PA_PWR_LVL register is 0x32, 35.8 mA
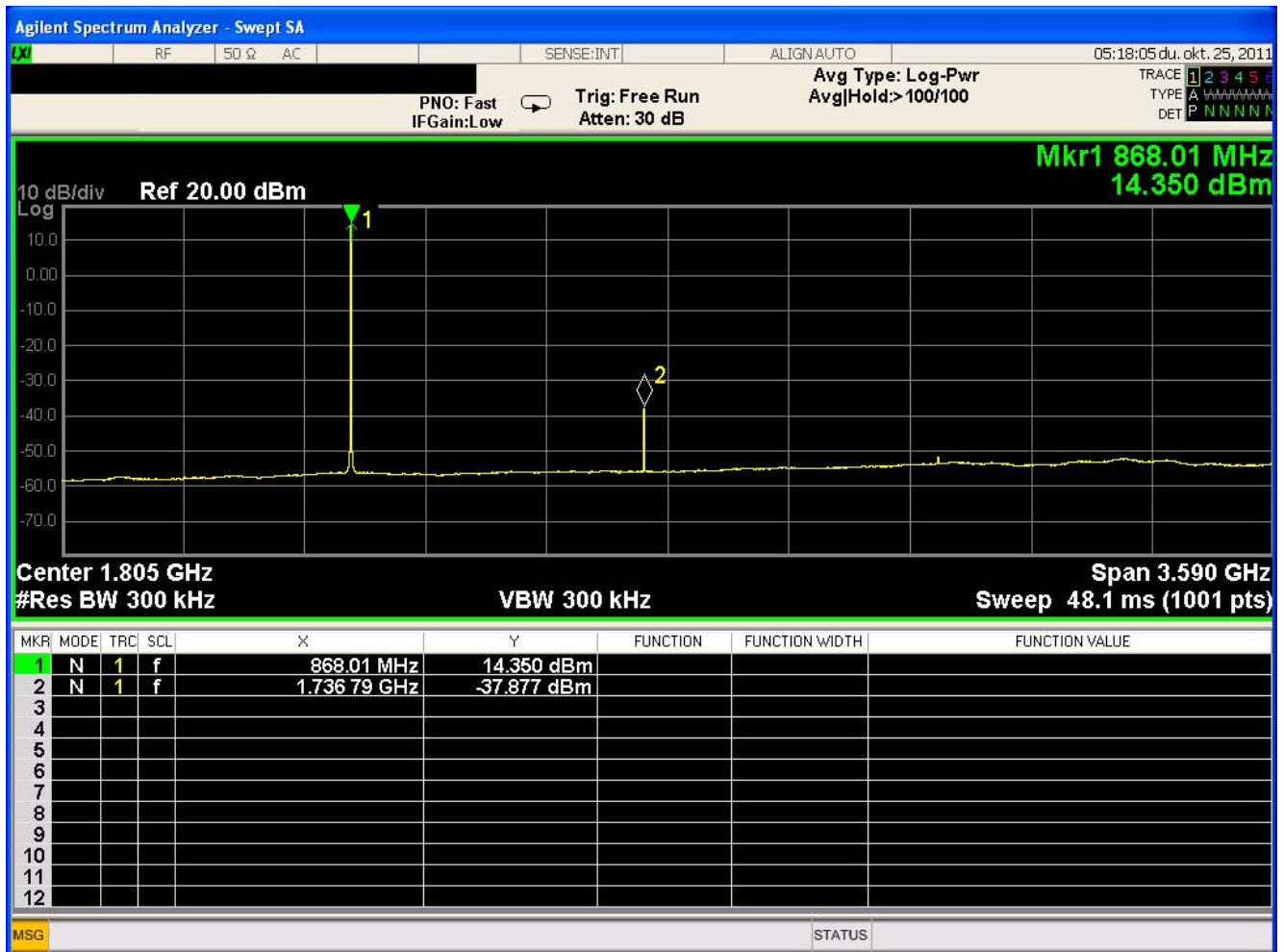
Figure 48. Si4461 14 dBm Split TX/RX Board at 868 MHz with Wire-Wound Inductors, V_DD = 3.2 V, DDAC[6:0] field in the PA_PWR_LVL register is 0x2B, 31.6 mA
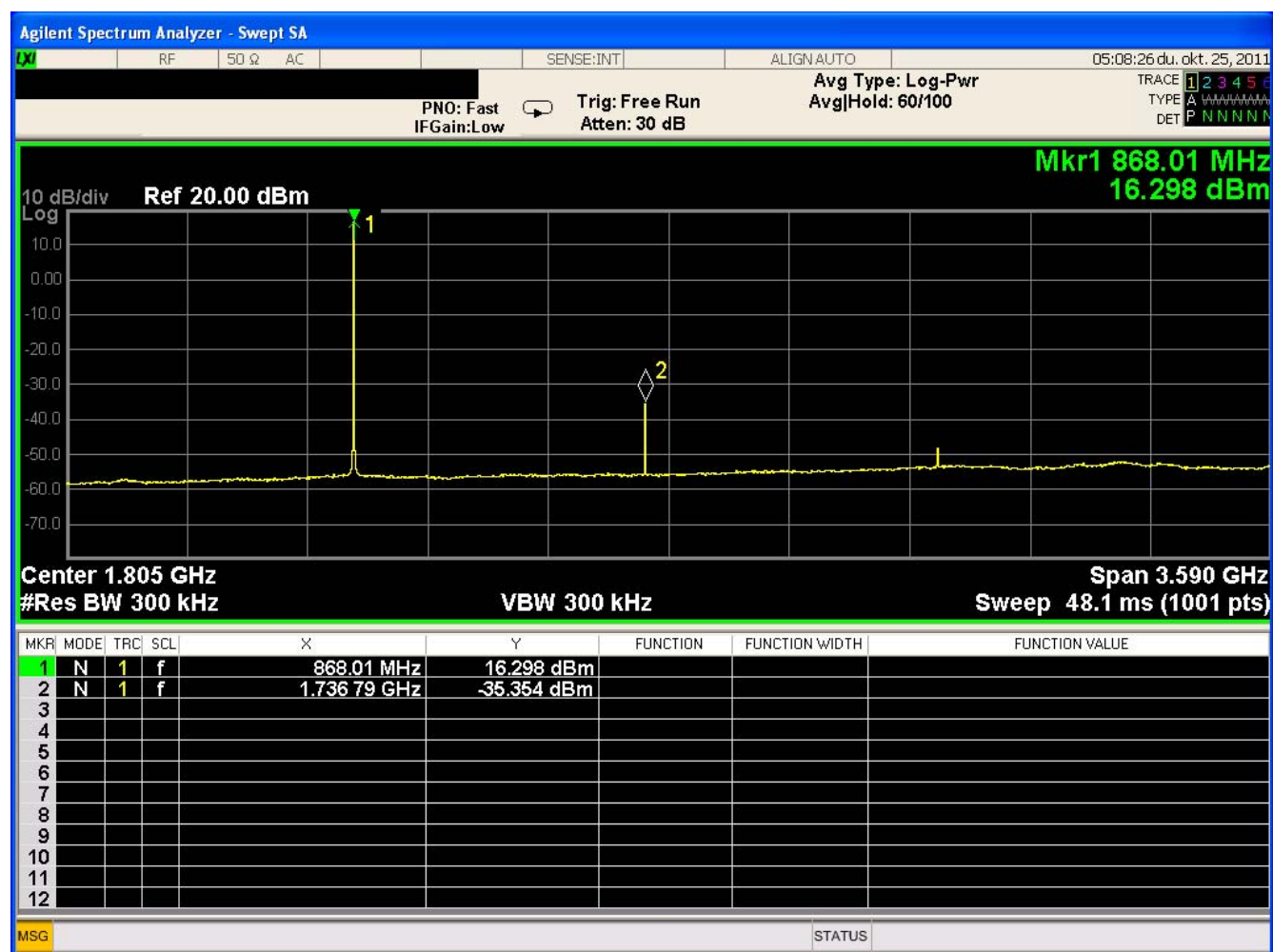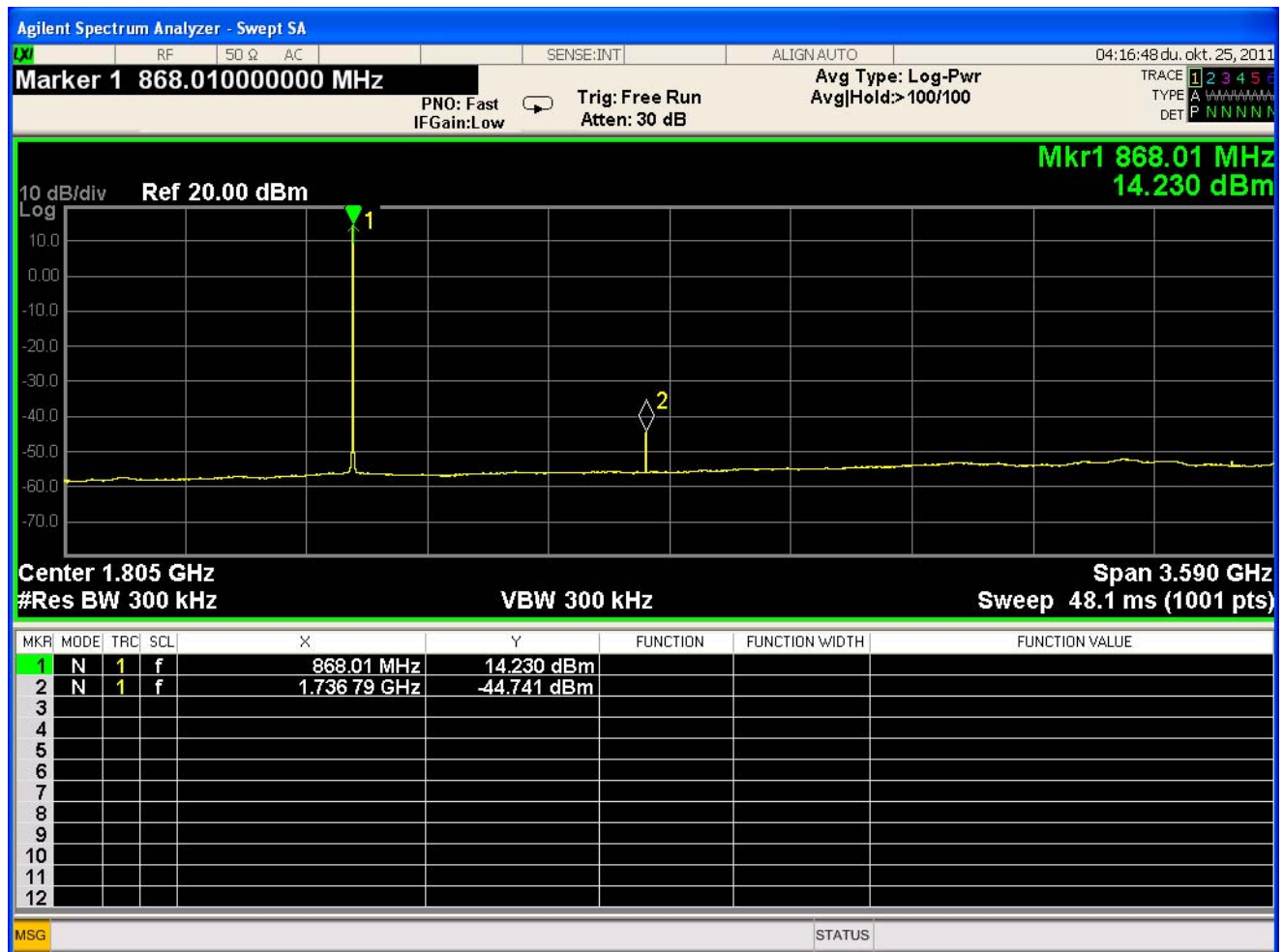
Figure 49. Si4461 16 dBm Split TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] field in the PA_PWR_LVL register is 0x40, 38.9 mA

Si4461 Split TX/RX Board CLE Configurations with Multilayer Inductors
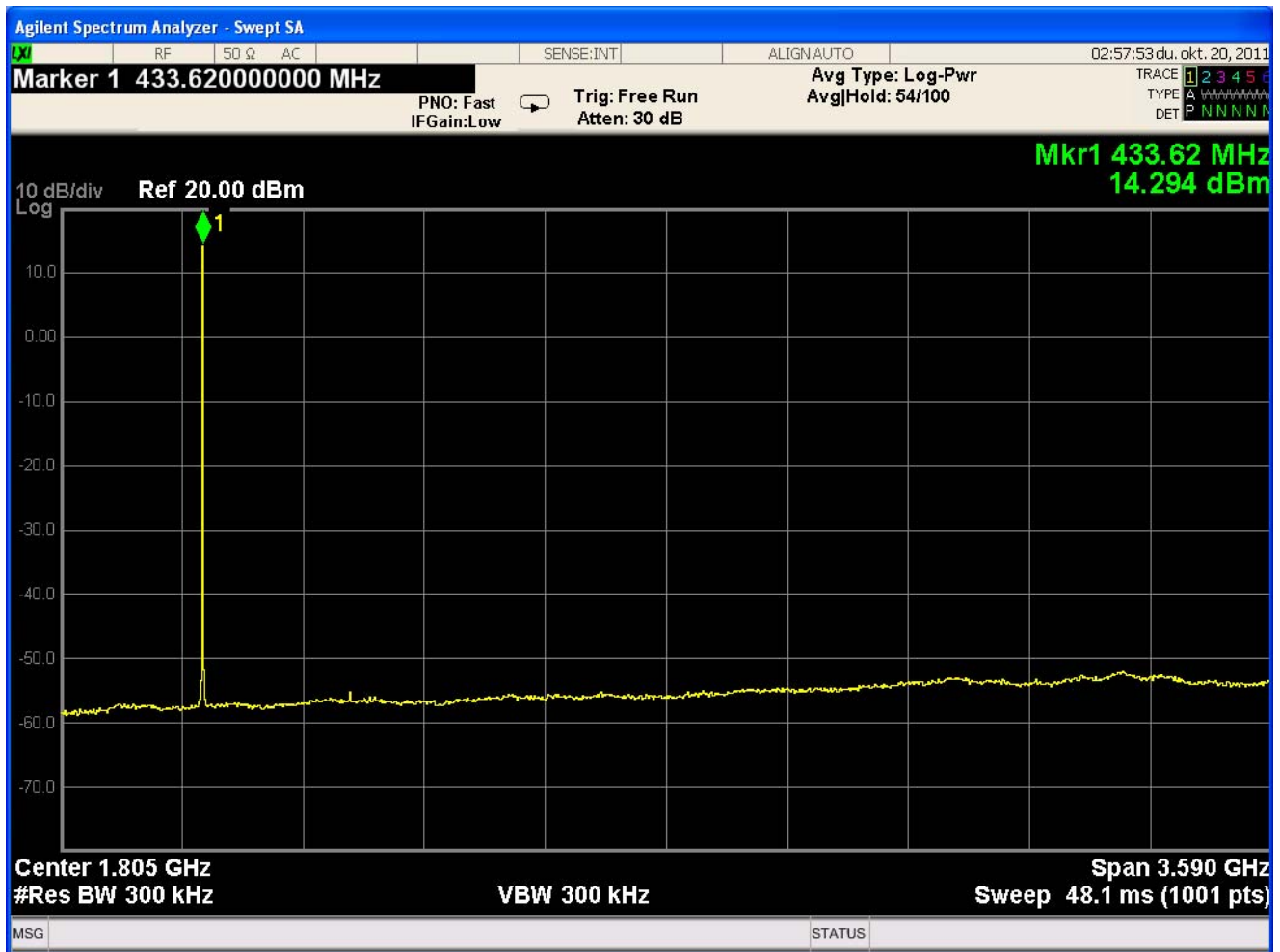
Figure 50. Si4461 14 dBm Split TX/RX Board at 434 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] field in the PA_PWR_LVL register is 0x2D, 29.7 mA
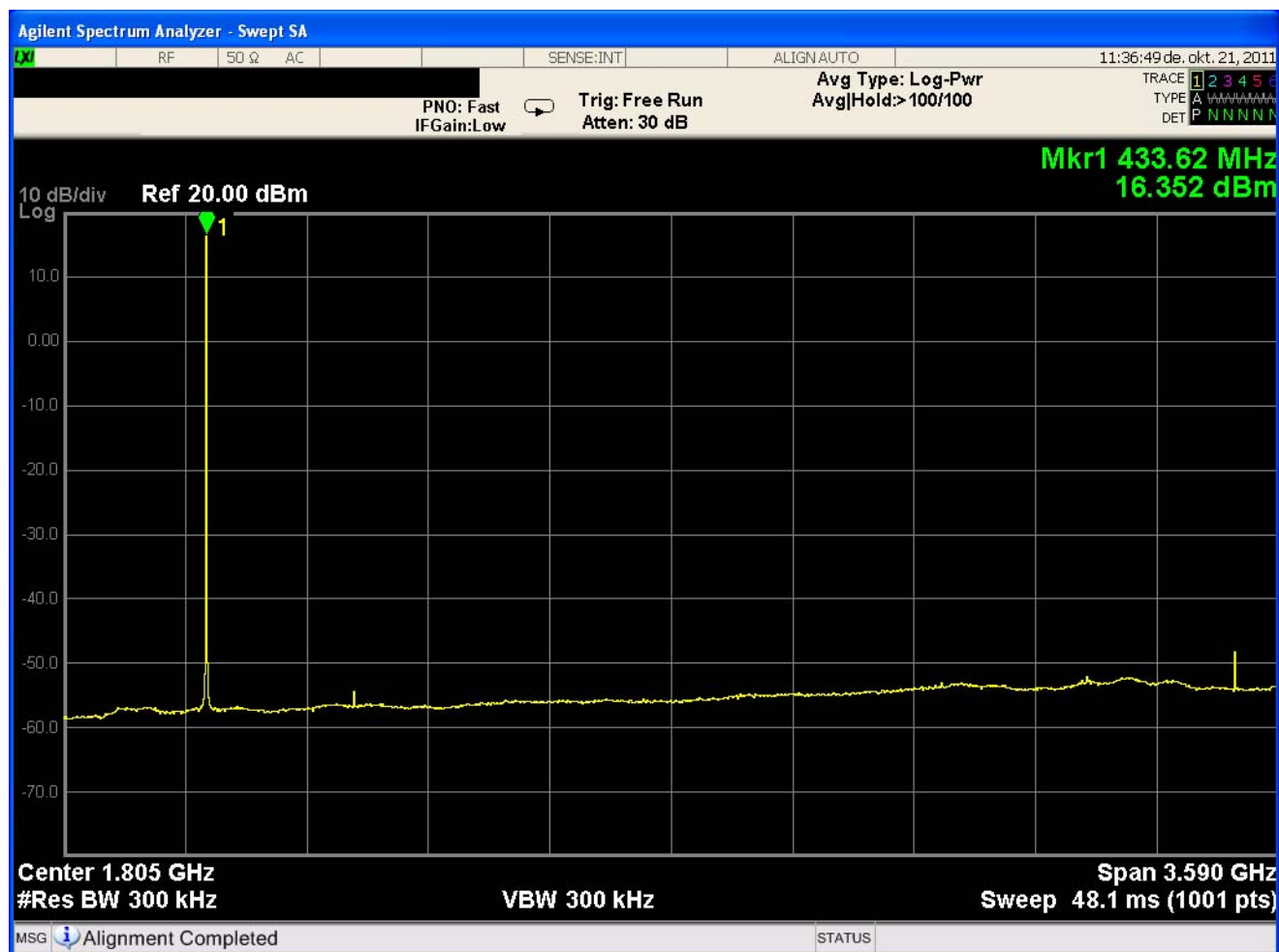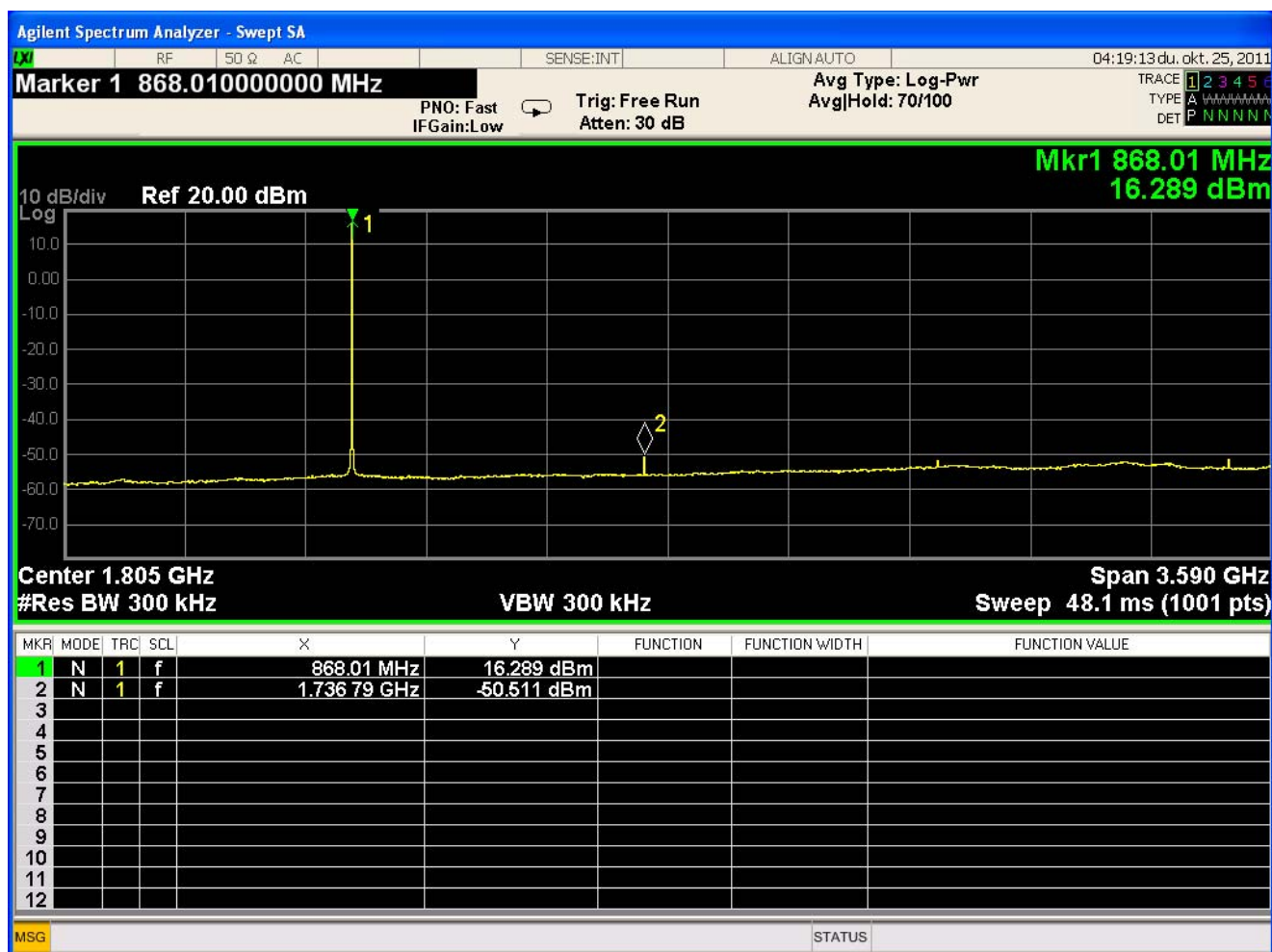
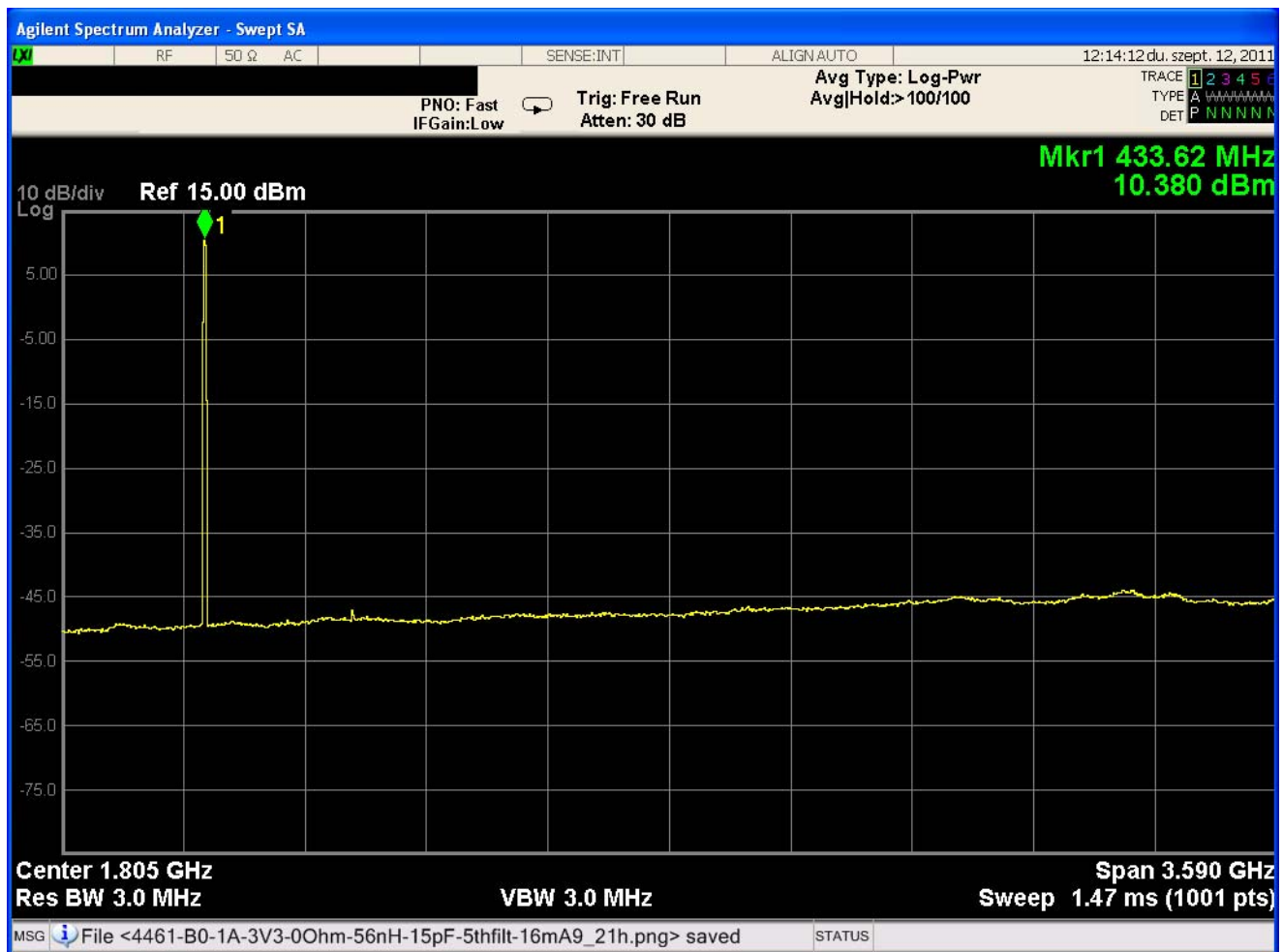**Figure 51. Si4461 16 dBm Split TX/RX Board at 434 MHz with Multilayer Inductors, V$_{DD}$ = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x7Fh, 38.9 mA**
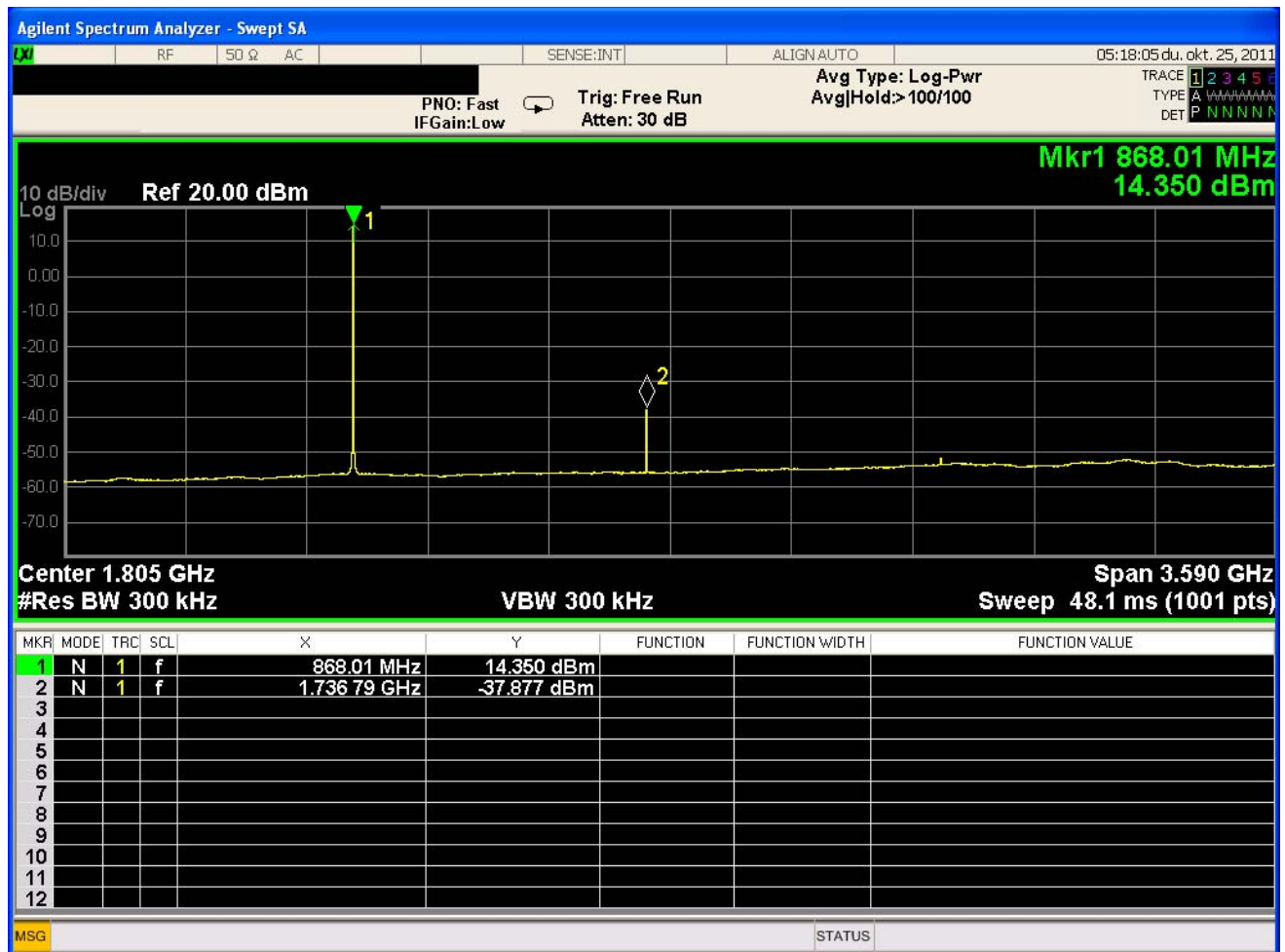
Figure 52. Si4461 14 dBm Split TX/RX Board at 868 MHz with Multilayer Inductors, V$_{DD}$ = 3.2 V, DDAC[6:0] field in the PA_PWR_LVL Register is 0x34, 34.4 mA
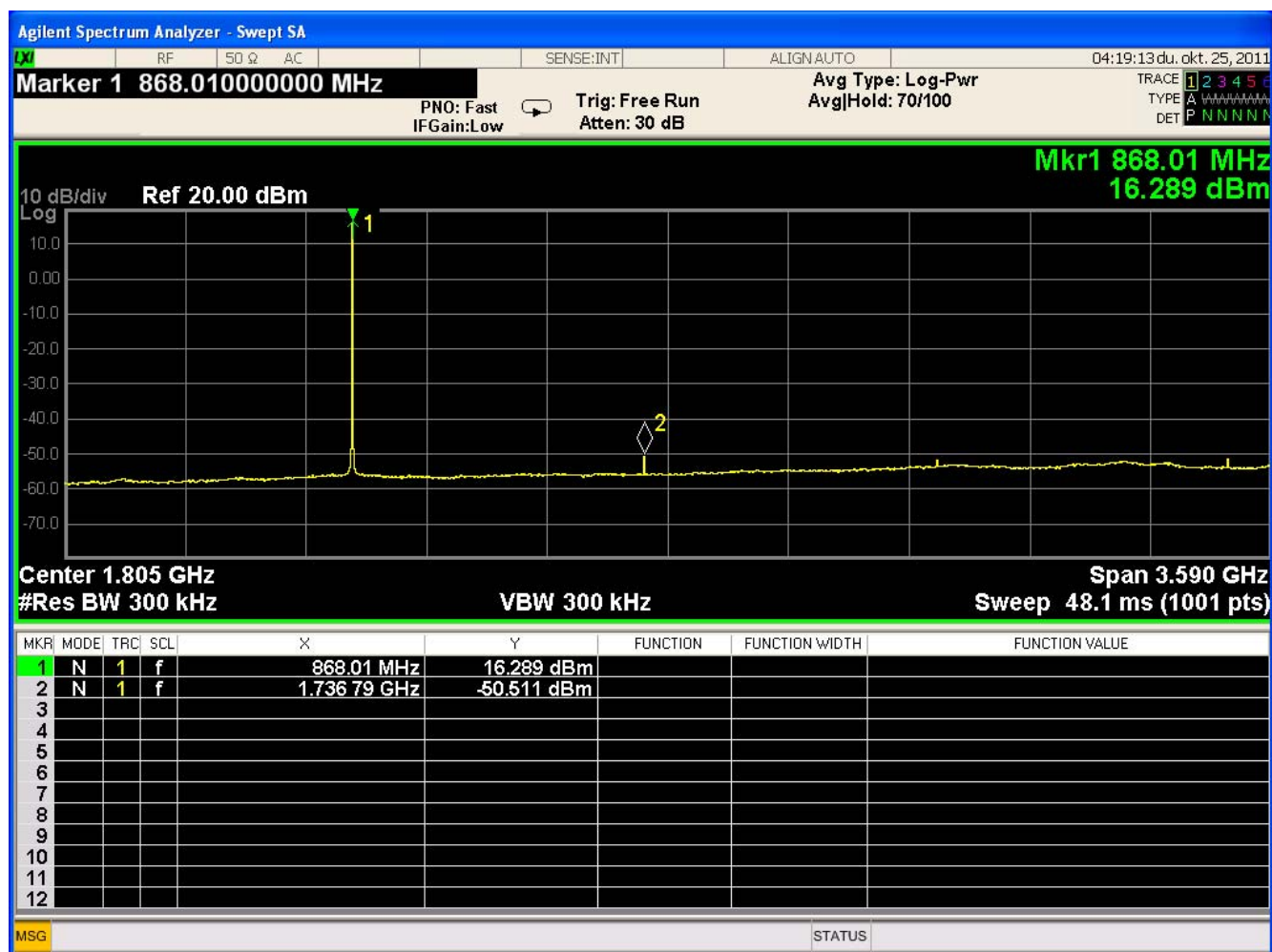
Figure 53. Si4461 16 dBm Split TX/RX Board at 868 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x4F, 42.7 mA

Si4461 Direct Tie TX/RX Board CLE Configurations with Wire-Wound Inductors
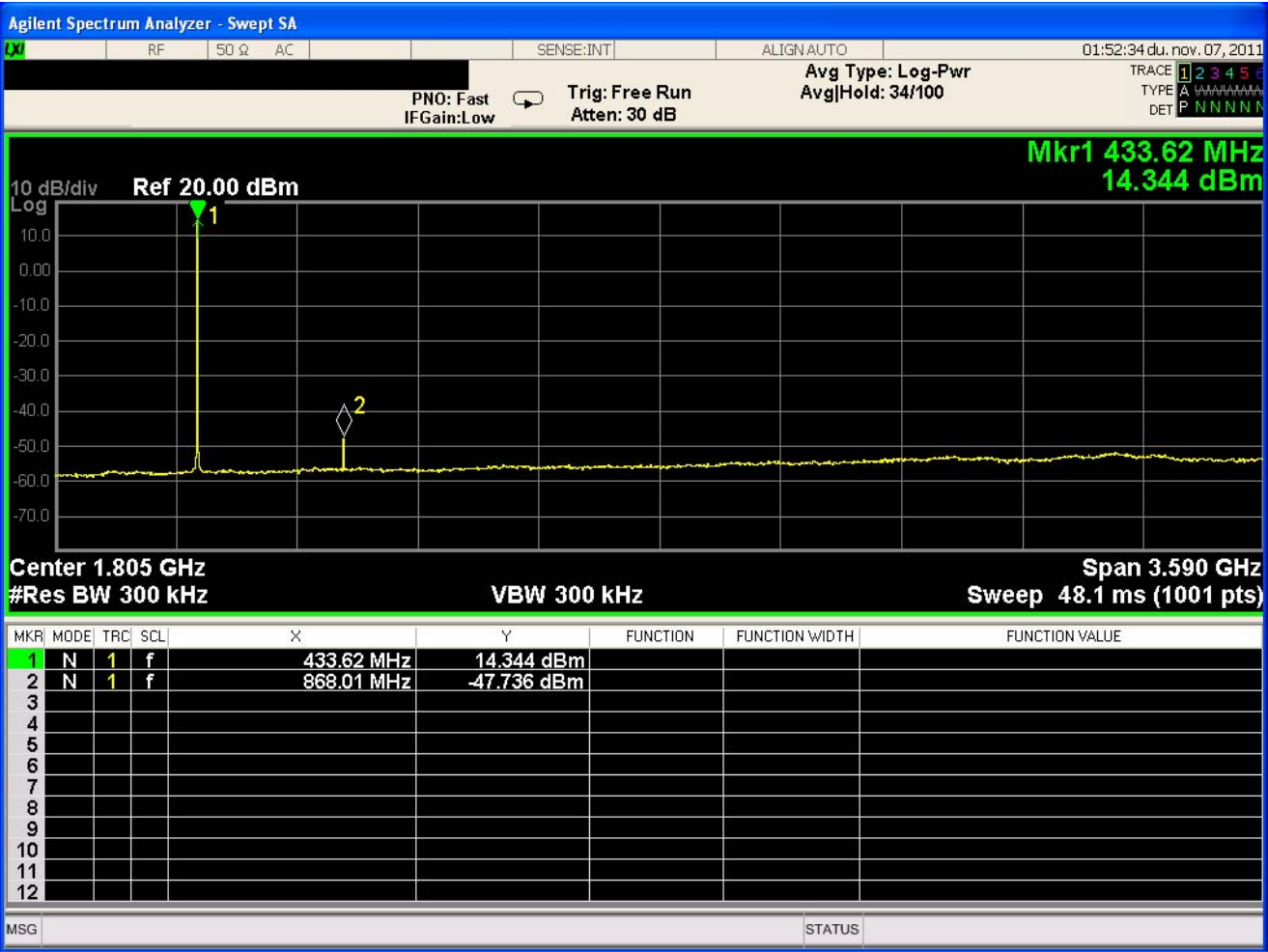
Figure 54. Si4461 14 dBm Direct Tie TX/RX Board at 434 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x21, 28.7 mA
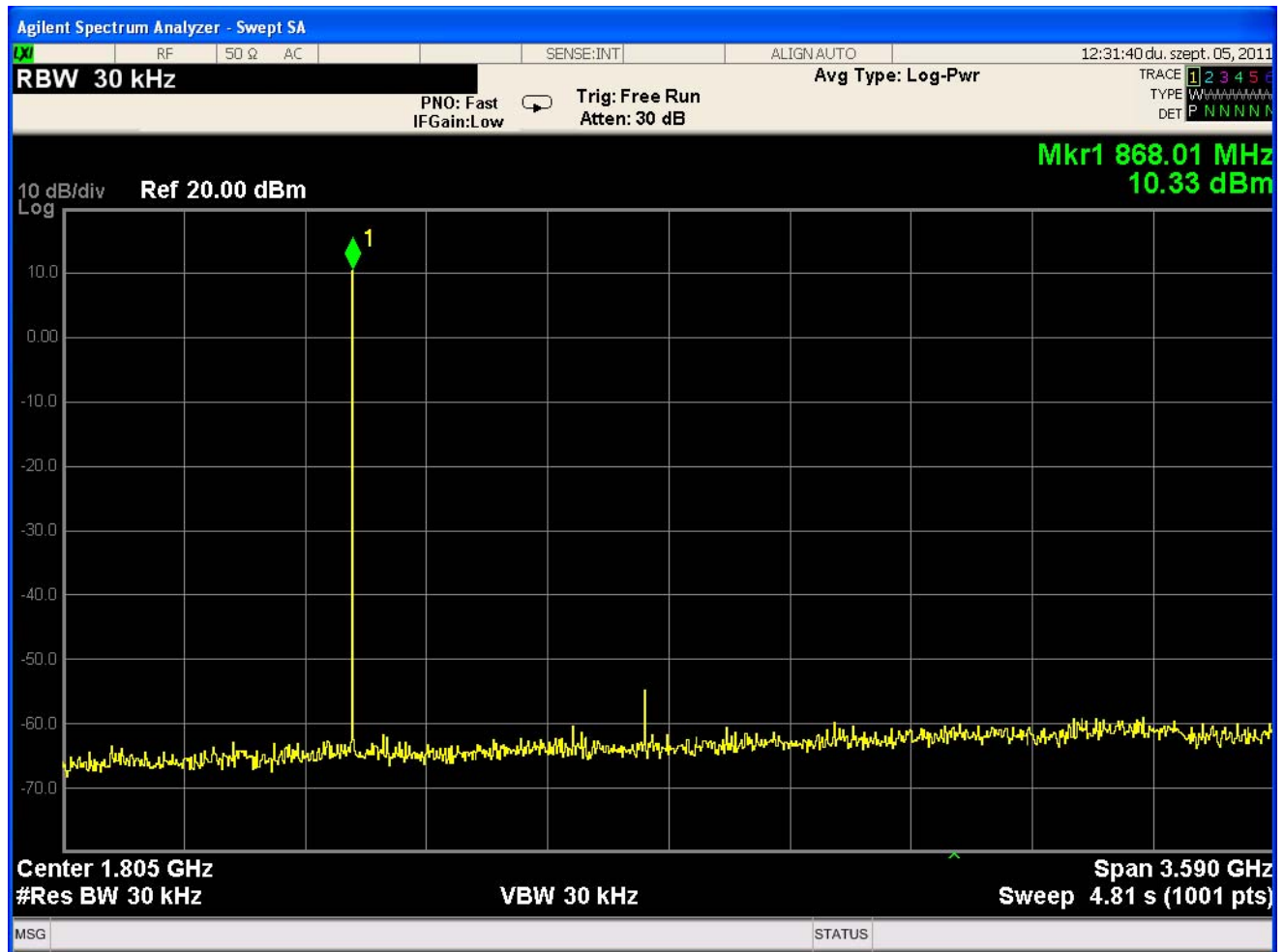
Figure 55. Si4461 16 dBm Direct Tie TX/RX Board at 434 MHz with Wire-Wound Inductors, V$_{DD}$ = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x31, 33 mA
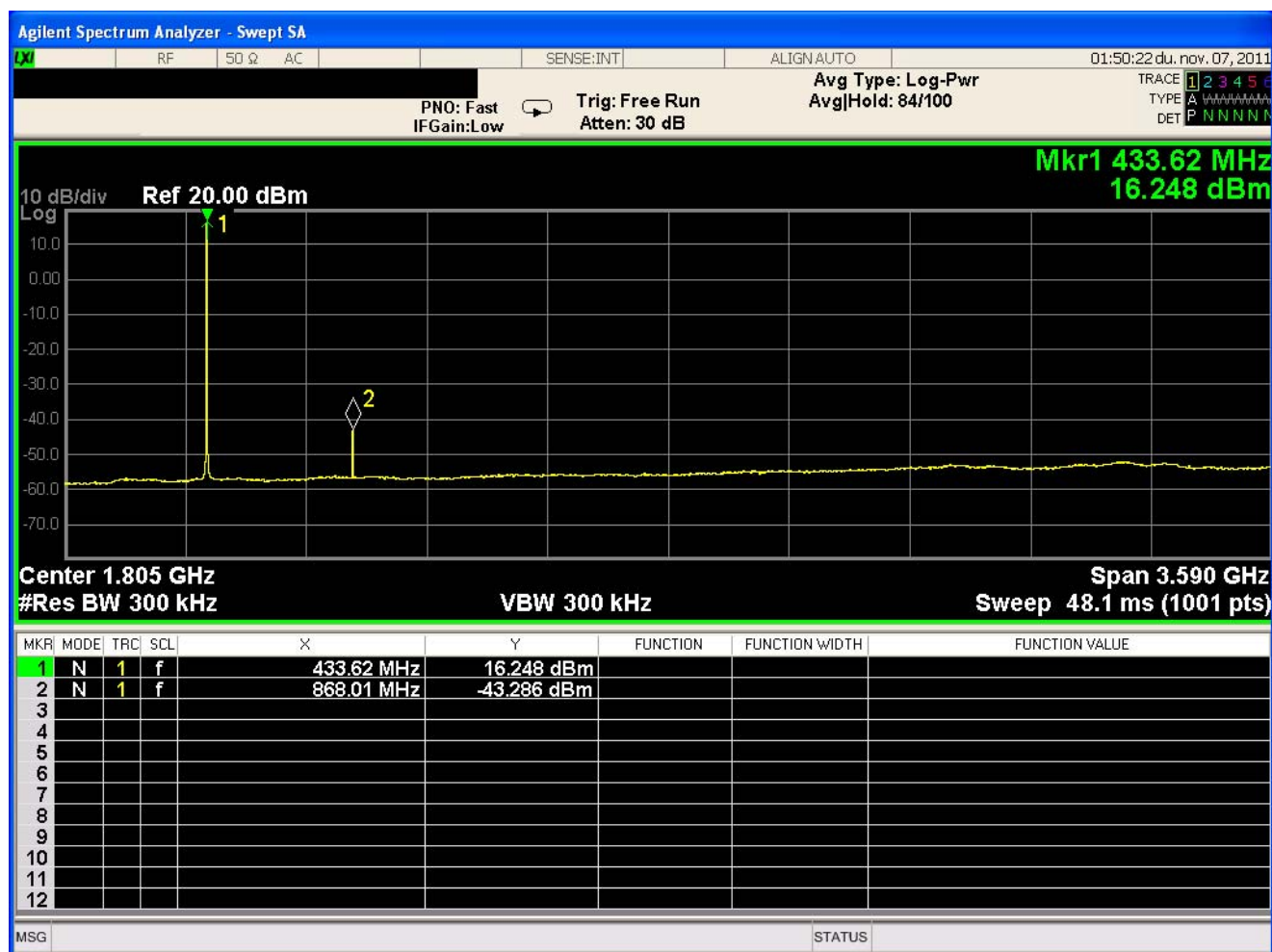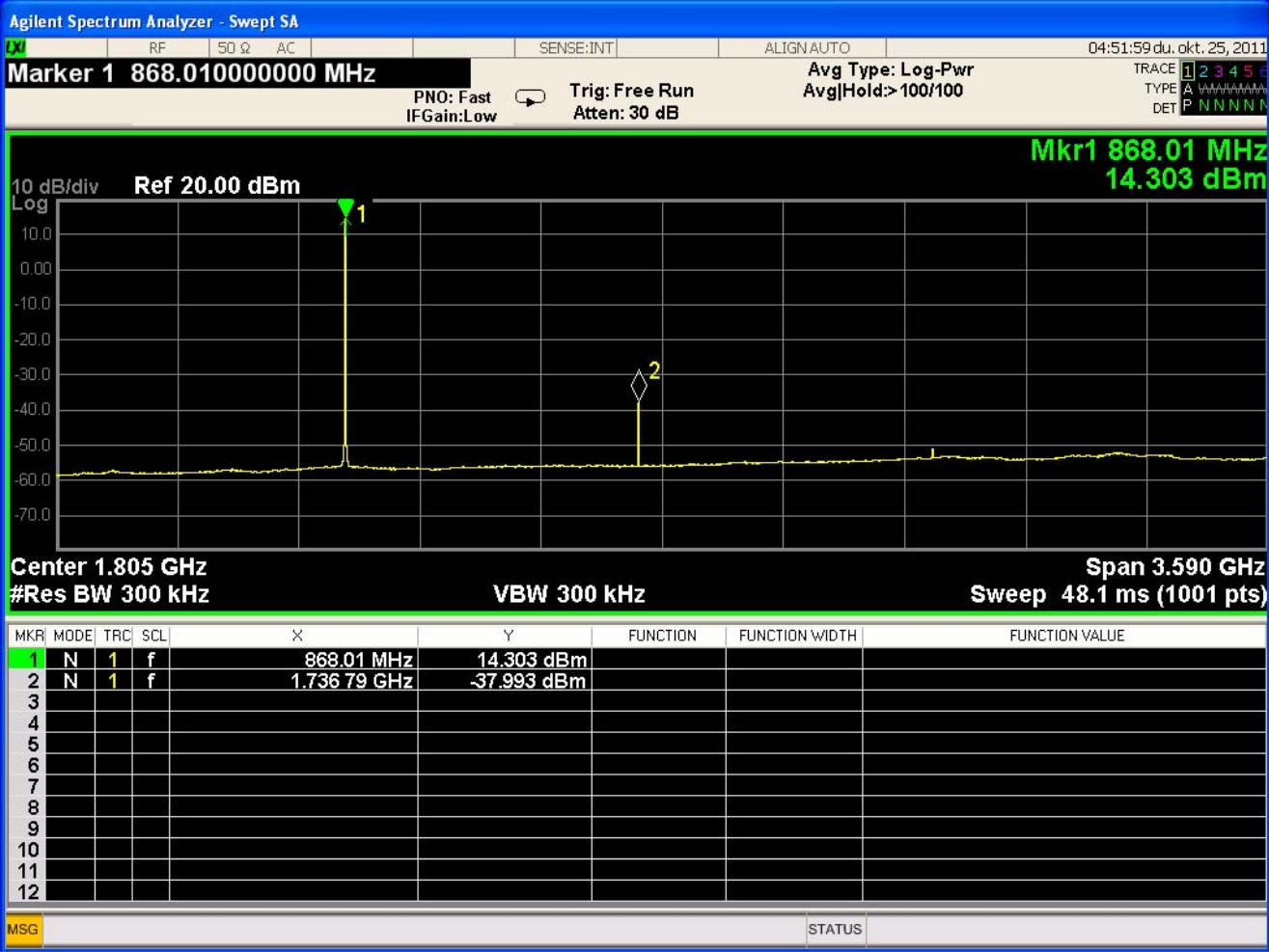
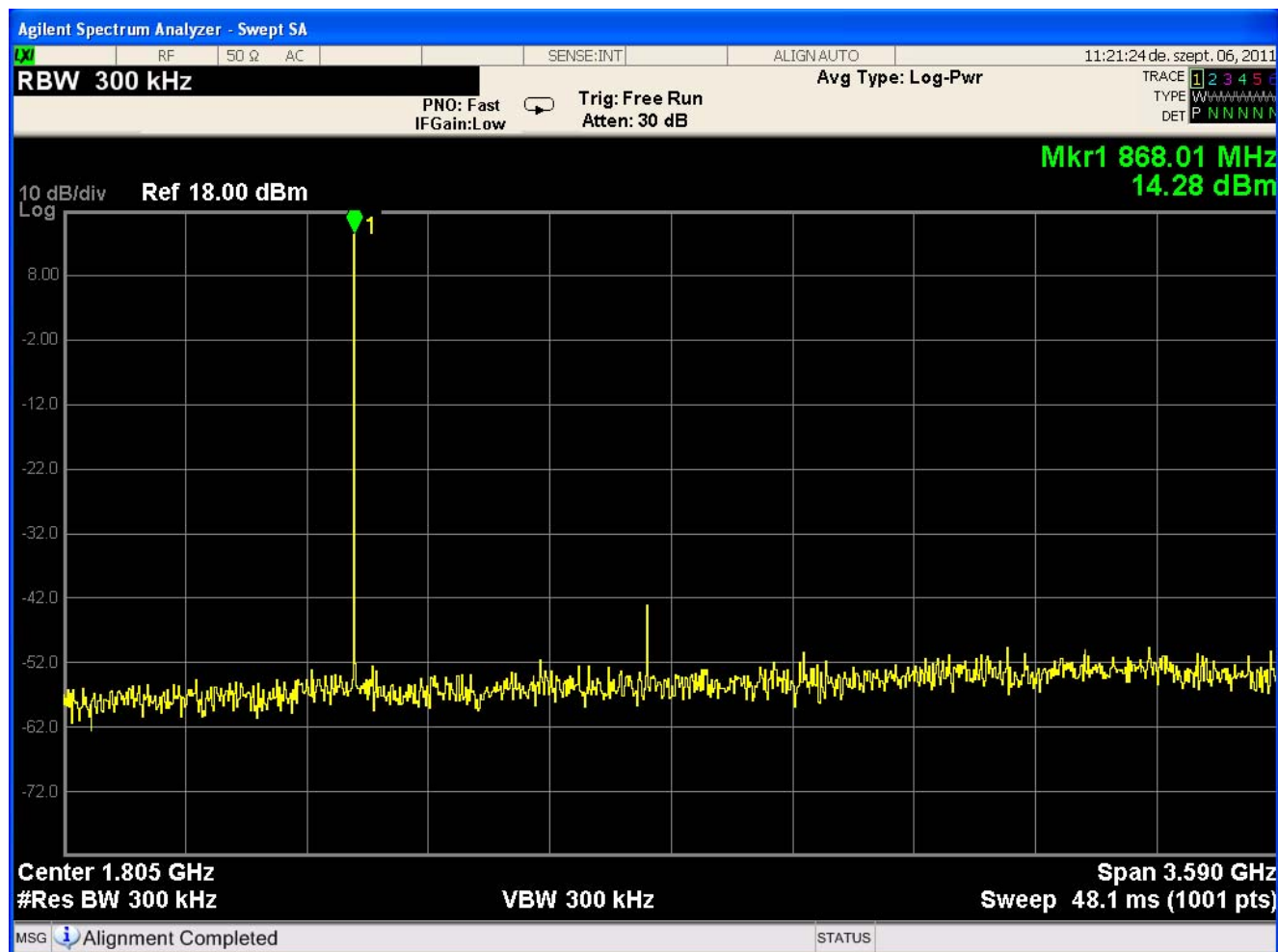**Figure 56. Si4461 14 dBm Direct Tie TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x2E, 33.2 mA**

Figure 57. Si4461 16 dBm Direct Tie TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] field in the PA_PWR_LVL Register is 0x41, 39.6 mA

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Si4461 Direct Tie TX/RX Board CLE Configurations with Multilayer Inductors

**Figure 58. Si4461 14 dBm Direct Tie TX/RX Board at 434 MHz with Multilayer Inductors,
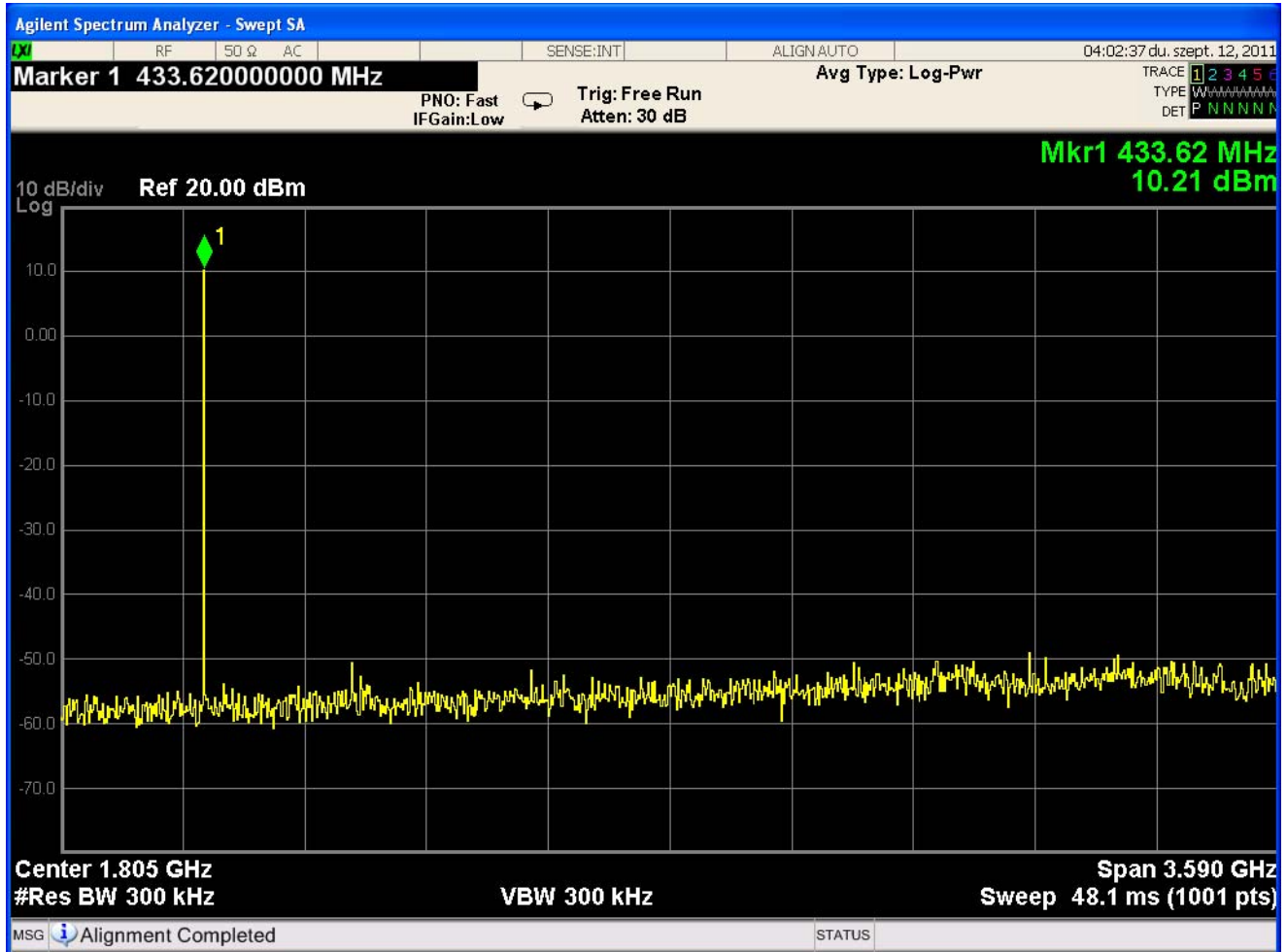VDD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x2F, 30.1 mA**

Figure 59. Si4461 16 dBm Direct Tie TX/RX Board at 434 MHz with Multilayer Inductors, V_{DD} = 3.2V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x7F, 40.1 mA

Figure 60. Si4461 14 dBm Direct Tie TX/RX Board at 868 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x34, 34.4 mA

Figure 61. Si4461 16dBm Direct Tie TX/RX Board at 868 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x5E, 42.9 mA

Si4060/Si4460/67 Measured Plots

Si4060/Si4460/67 Split TX/RX Board CLE Configurations with Wire-Wound Inductors

Figure 62. Si4060/Si4460/67 10 dBm Split TX/RX Board at 434 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x19, 16.9 mA
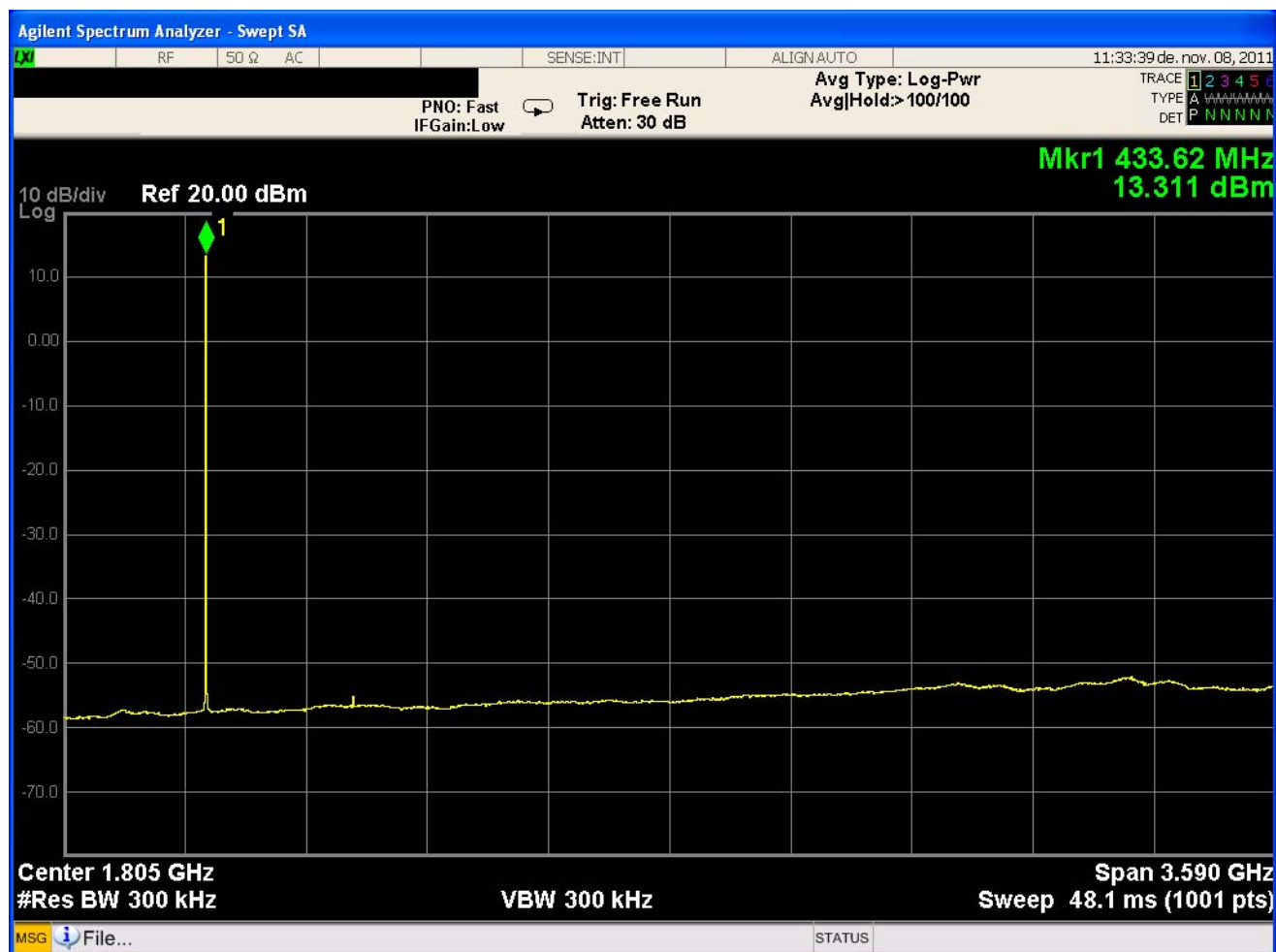
Figure 63. Si4060/Si4460/67 13 dBm Split TX/RX Board at 434 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x3F, 22.7 mA
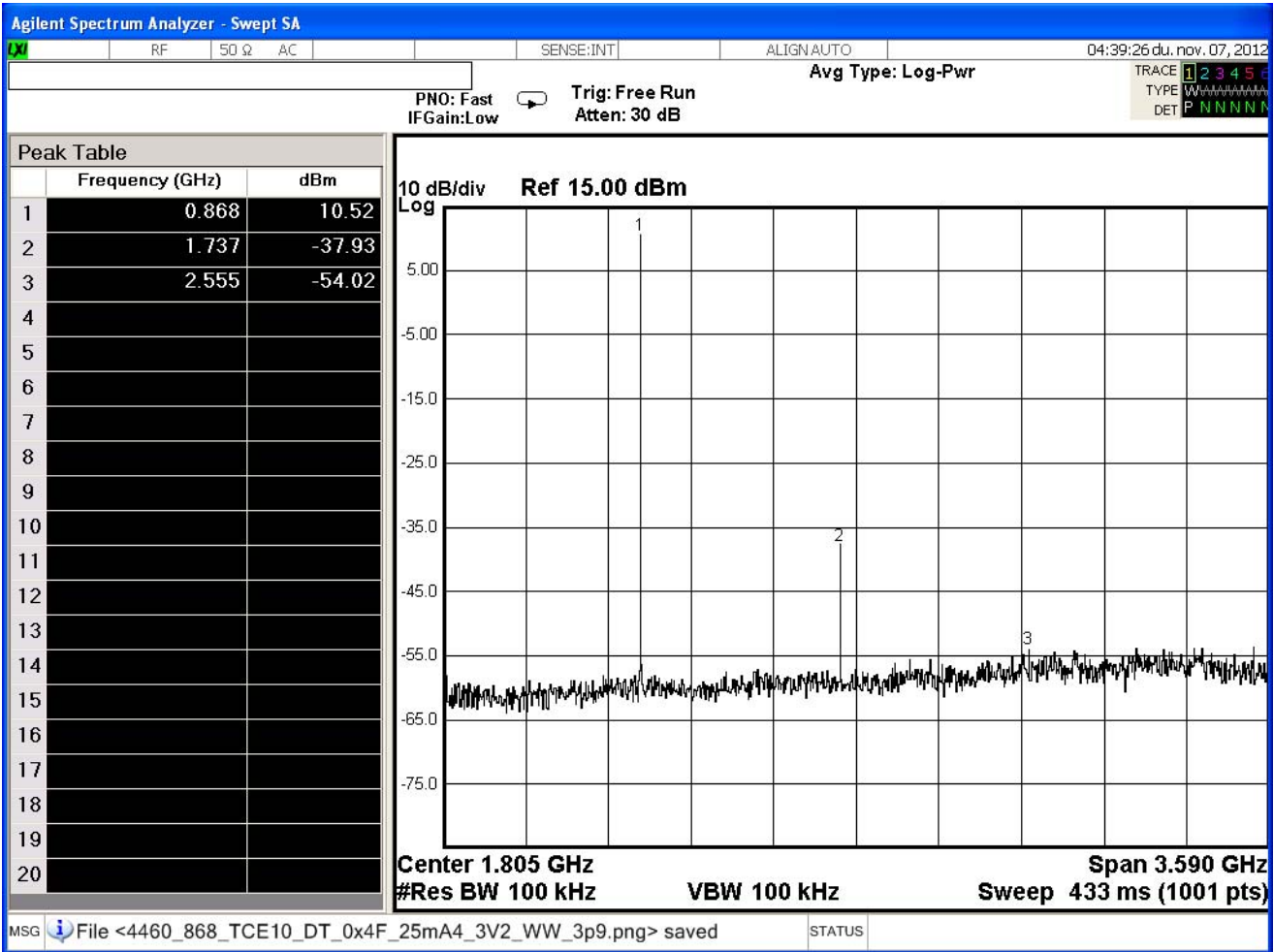
Figure 64. Si4060/Si4460/67 10 dBm Split TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x19h, 16.4 mA
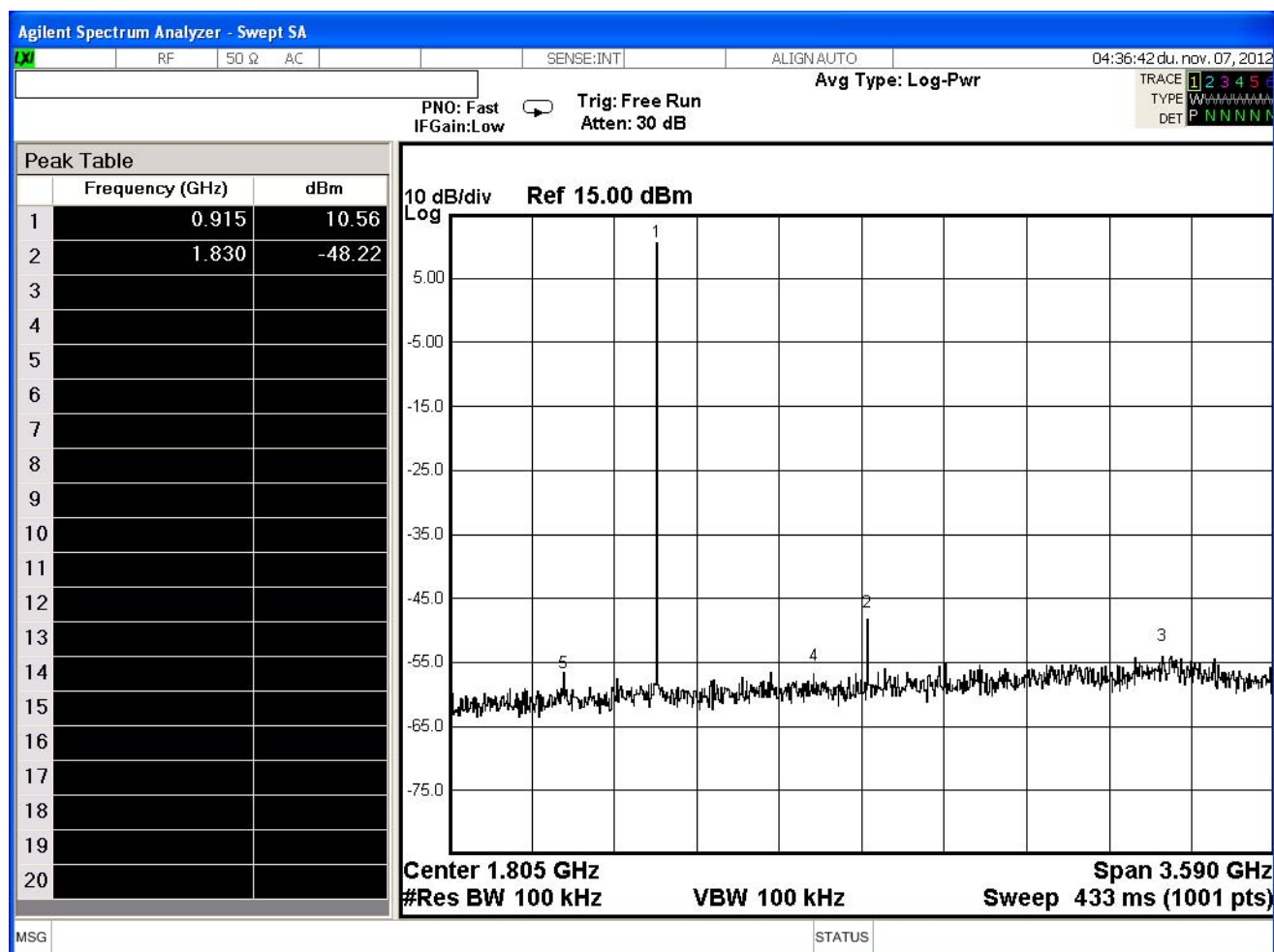
Figure 65. Si4060/Si4460/67 14 dBm Split TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x3Dh, 24.8 mA

Si4060/Si4460/67 Split TX/RX Board CLE Configurations with Multilayer Inductors

For Si4060/Si4460/67 Multilayer split TX/RX boards pls. use the TX part of the DT multilayer matches. The resulted spectrum plots are very close to that given for the multilayer DT boards in TX mode (pls. see 6.3.4 chapter).

Si4460/67 Direct Tie TX/RX Board CLE Configurations with Wire-Wound Inductors

Figure 66. Si4460/67 10 dBm Direct Tie TX/RX Board at 434 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x1A, 16.9 mA

Figure 67. Si4460/67 13 dBm HP Direct Tie TX/RX Board at 434 MHz with Wire-Wound Inductors, V$_{DD}$ = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x3F, 23 mA

Figure 68. Si4460/67 10 dBm 868–915M Direct Tie TX/RX Board at 868 MHz with Wire-Wound Inductors, V_DD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x20, 19.7 mA
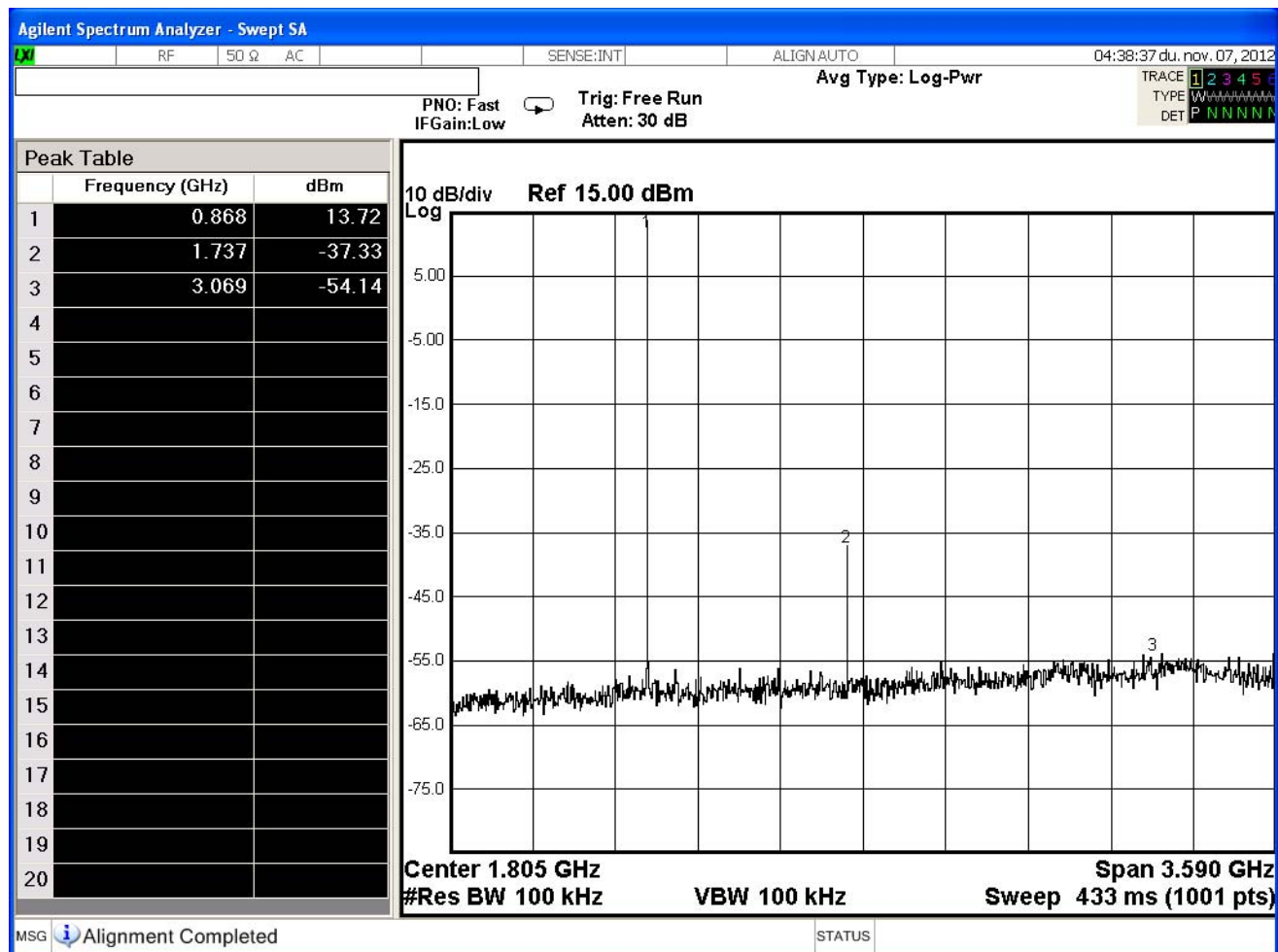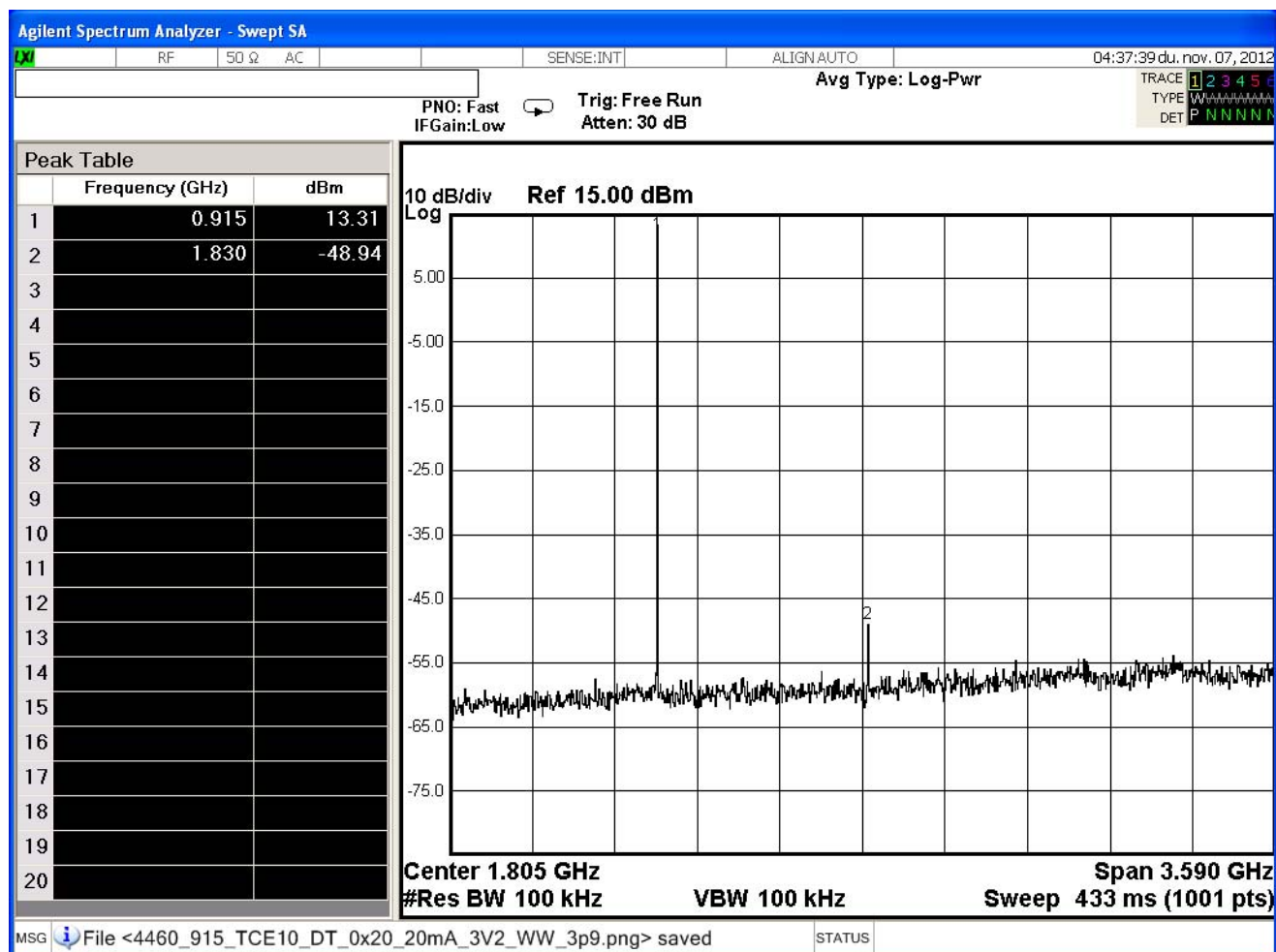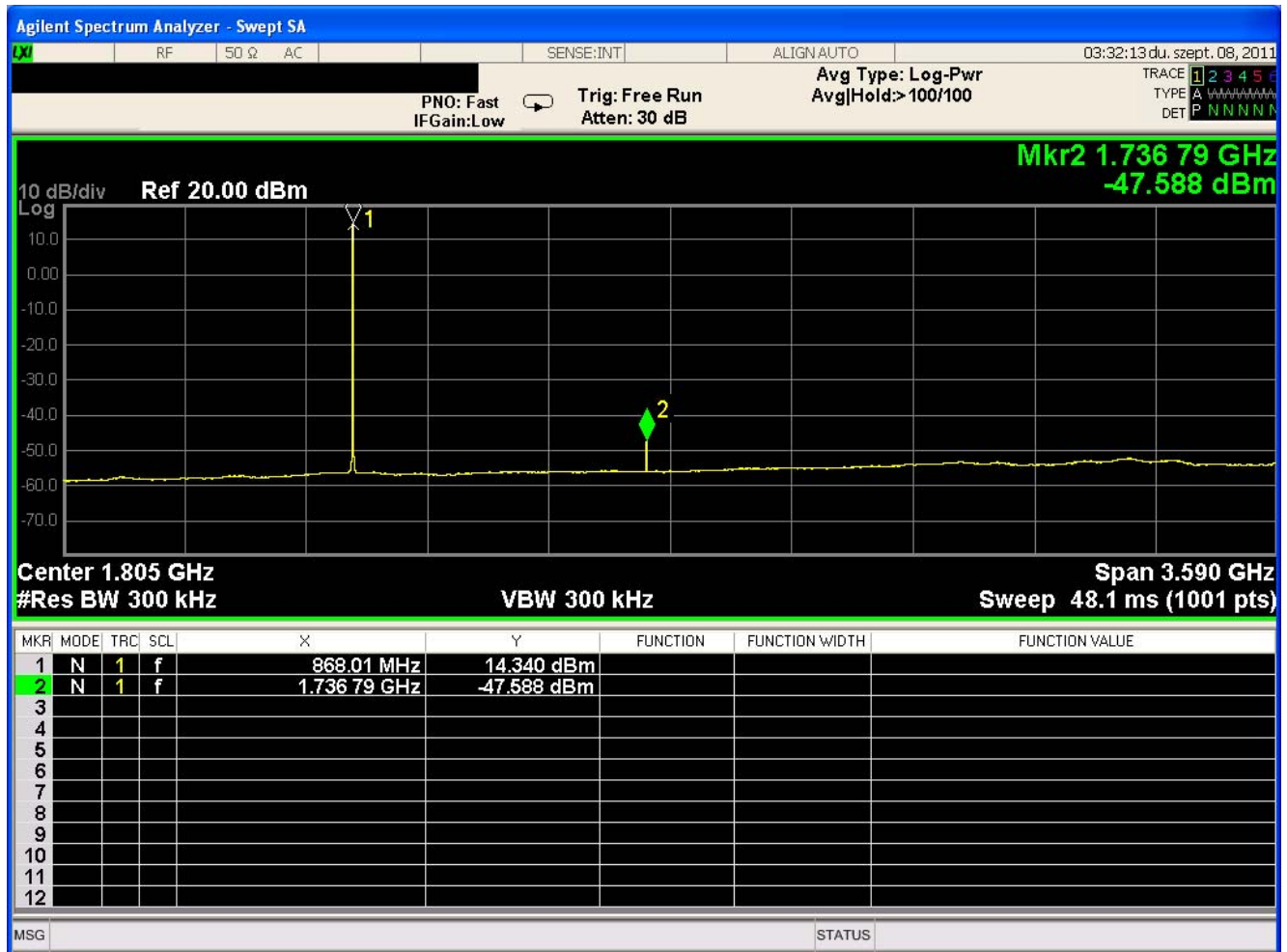
Figure 69. Si4460/67 10 dBm 868–915M Direct Tie TX/RX Board at 915 MHz with Wire-Wound Inductors, VDD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x20, 20 mA

Figure 70. Si4460/67 868-915M Direct Tie TX/RX Board at 868 MHz at Max Power State with Wire-Wound Inductors, VDD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x4F, 25.5 mA

Figure 71. Si4460/67 868–915M Direct Tie TX/RX Board at 915 MHz at Max Power State with Wire-Wound Inductors, VDD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x4F, 24.7 mA

Figure 72. Si4460/67 14 dBm Direct Tie HP TX/RX Board at 868 MHz with Wire-Wound Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x44, 25.6 mA

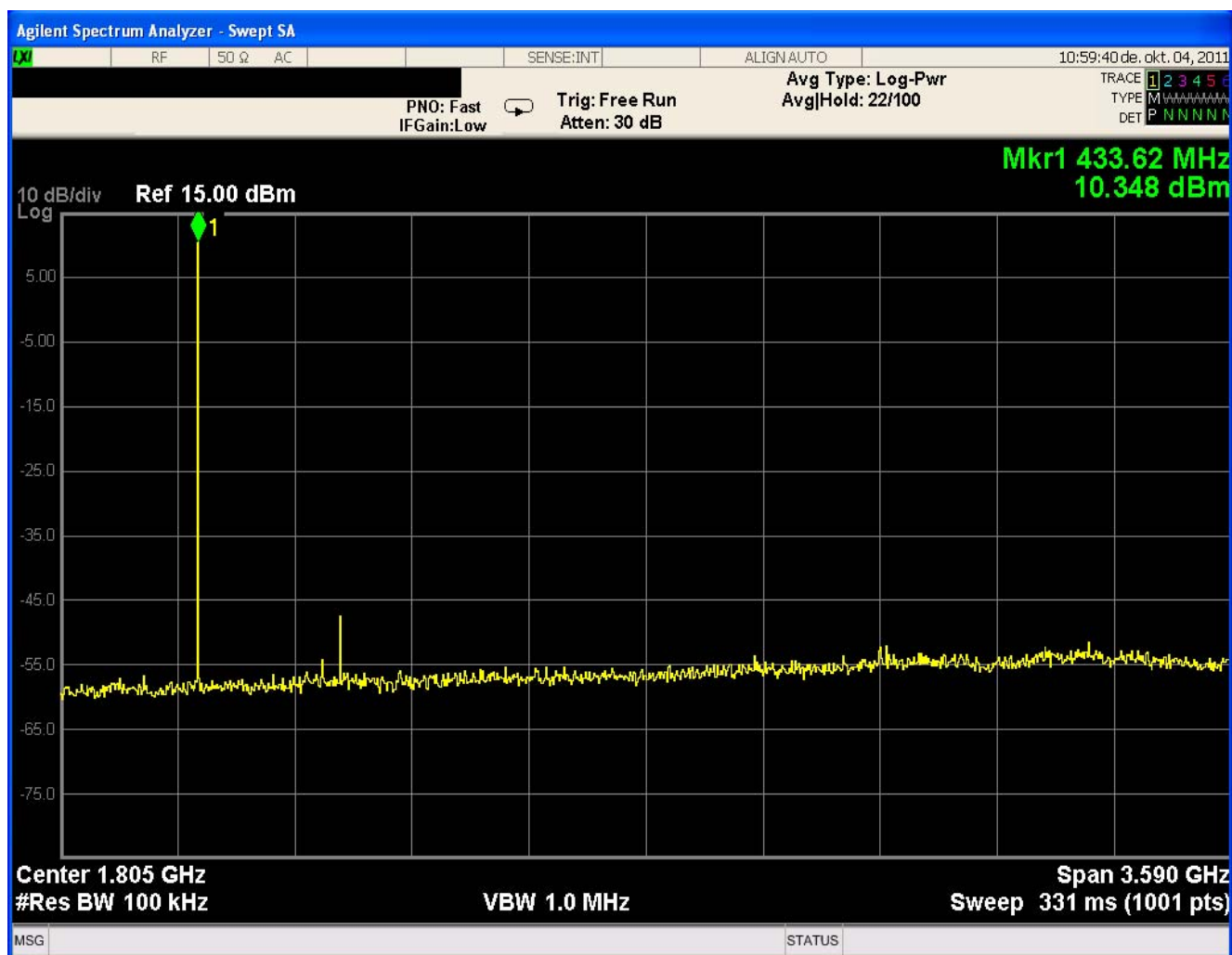**Si4460/67 Direct Tie TX/RX Board CLE Configurations with Multilayer Inductors**

Figure 73. Si4460/67 10 dBm Direct Tie TX/RX Board at 434 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x2A, 17.1 mA
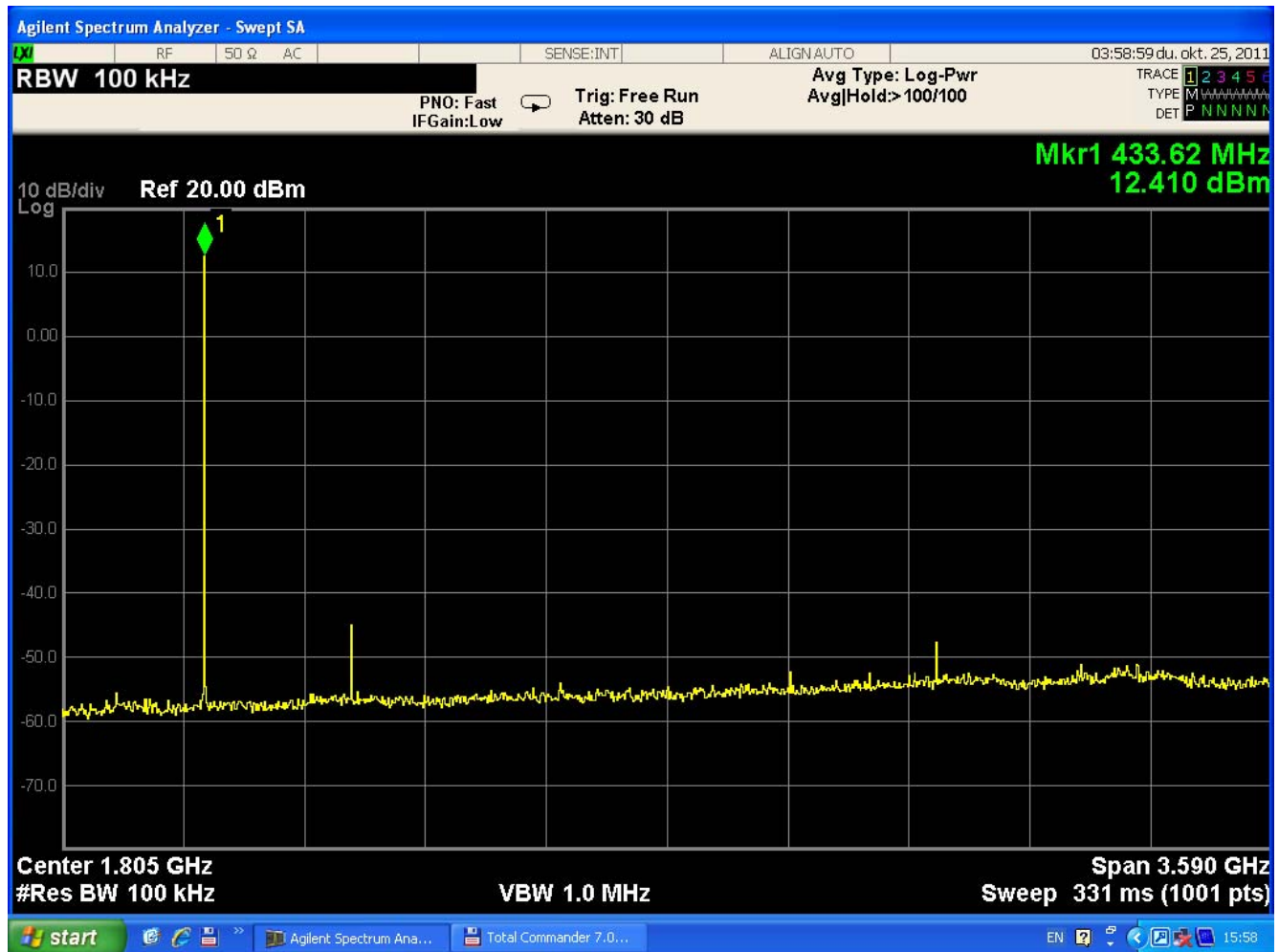
Figure 74. Si4460/67 12.3 dBm Direct Tie HP TX/RX Board at 434 MHz with Multilayer Inductors, V$_{DD}$ = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x4F, 23.1 mA
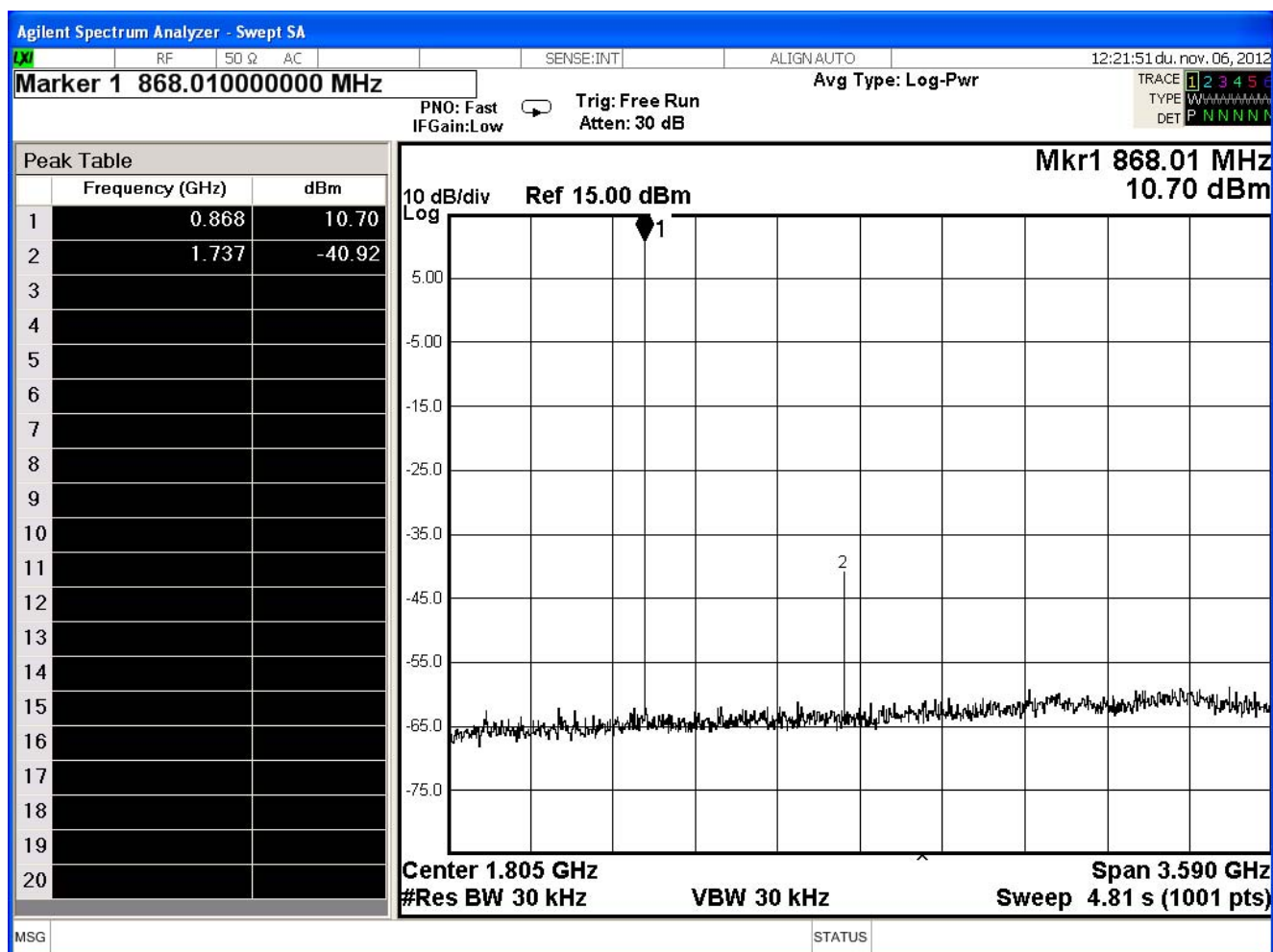
Figure 75. Si4460/67 10 dBm 868–915M Direct Tie TX/RX Board at 868 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x20, 19.7 mA
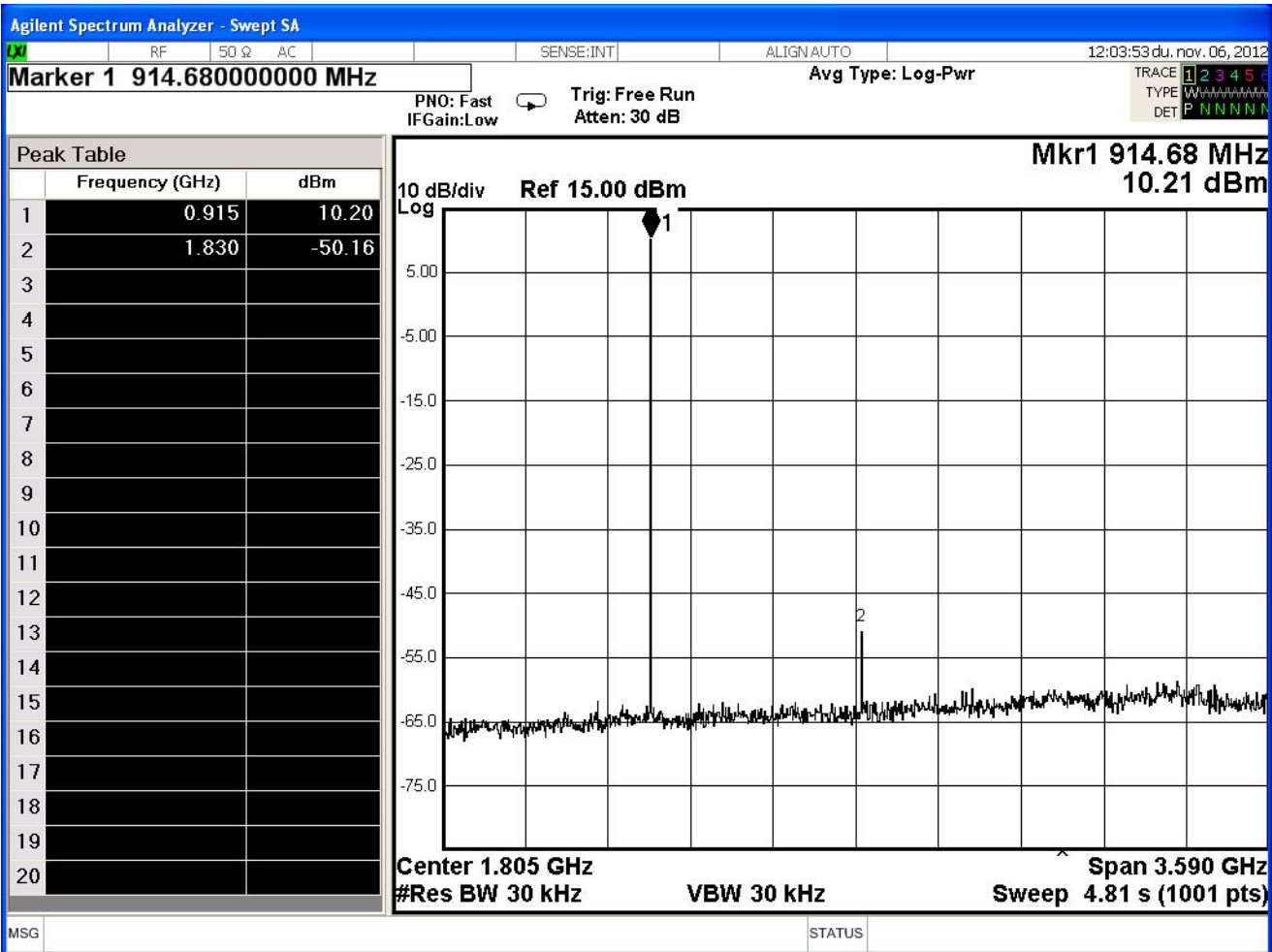
Figure 76. Si4460/67 10 dBm 868–915M Direct Tie TX/RX Board at 915 MHz with Wire-Wound Inductors, VDD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x20, 19.3 mA
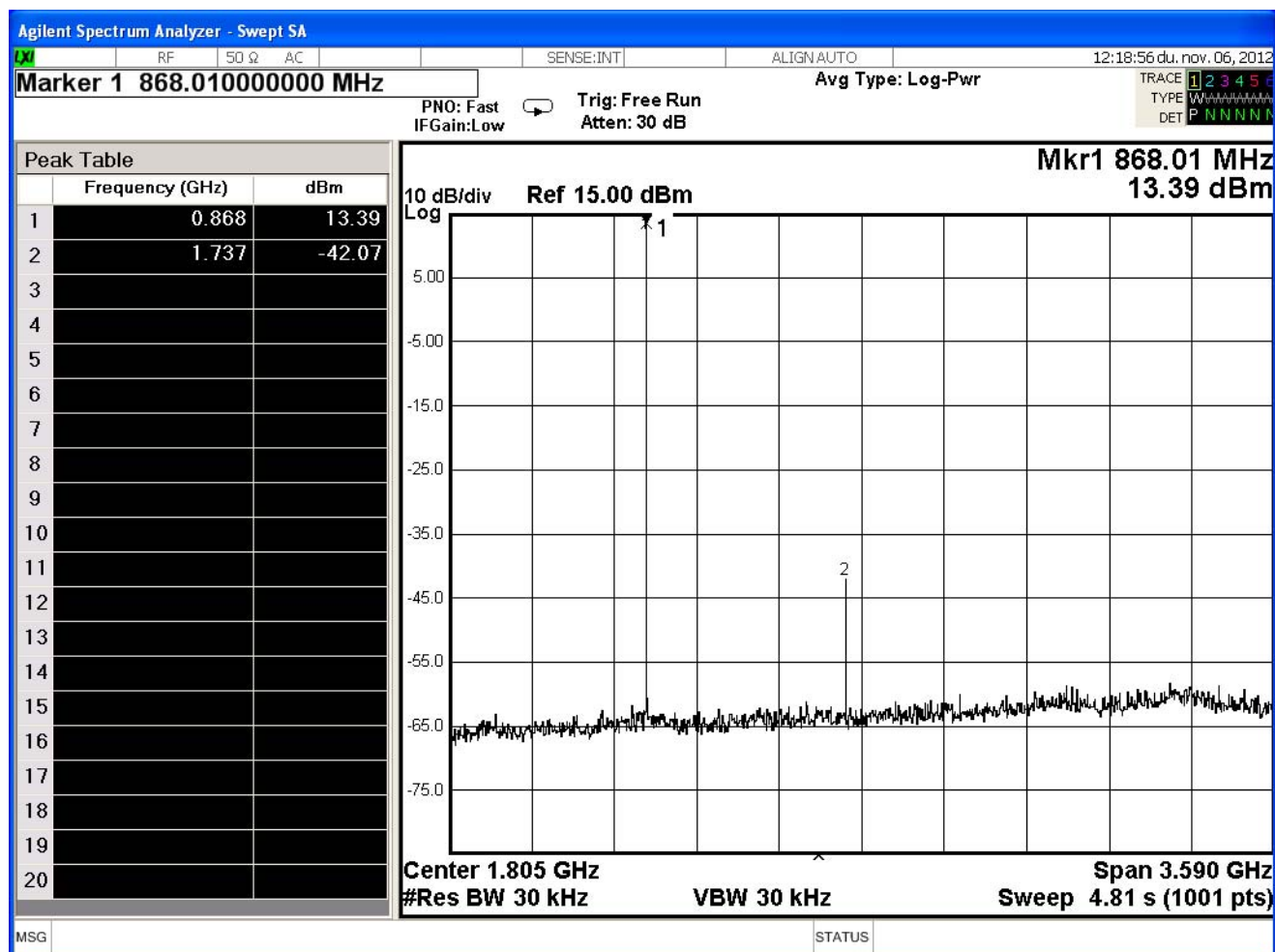
Figure 77. Si4460/67 868–915M Direct Tie TX/RX Board at 868 MHz at Max Power State with Multilayer Inductors, VDD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x4F, 24.7 mA
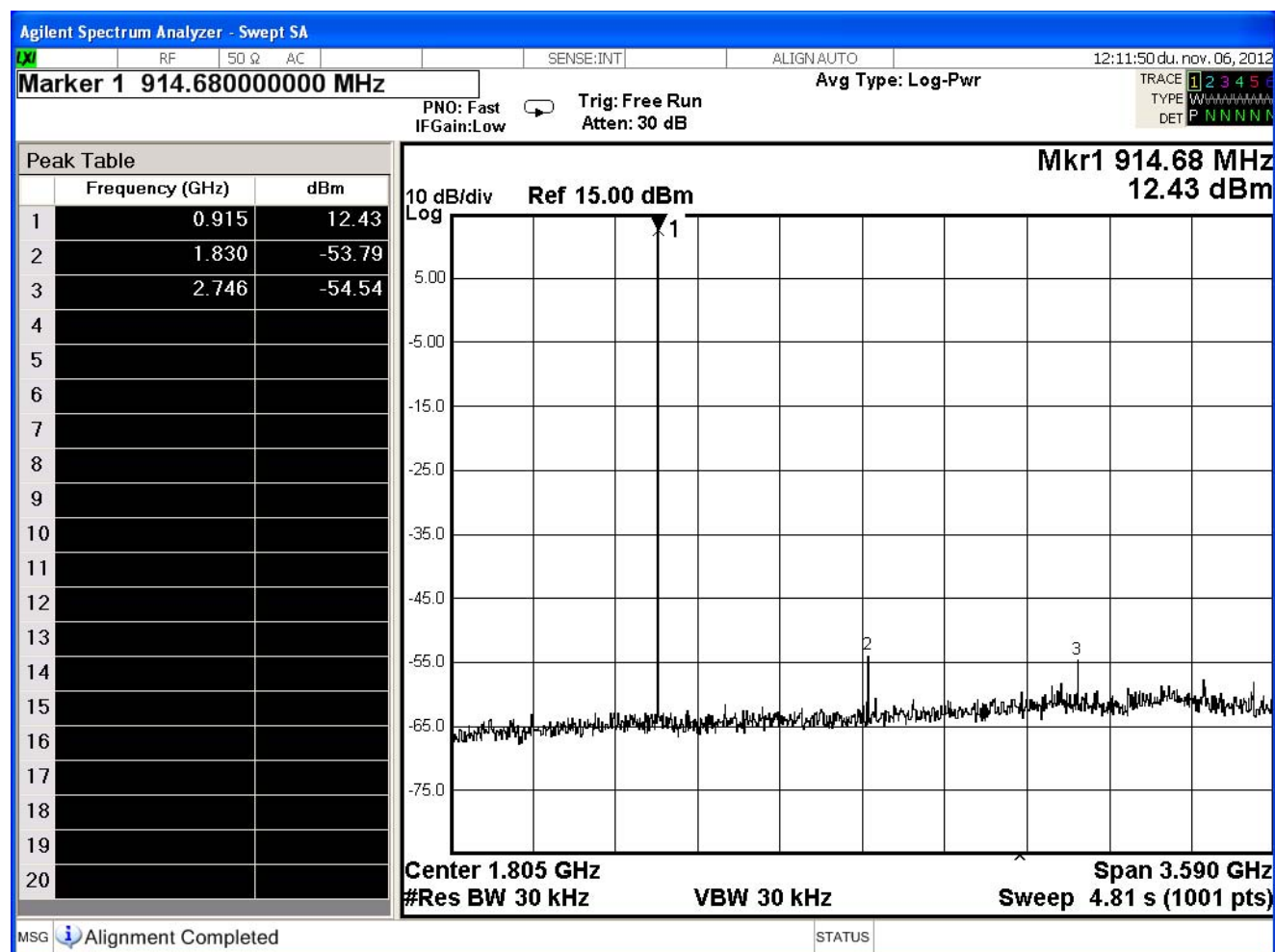
Figure 78. Si4460/67 868–915M Direct Tie TX/RX Board at 915 MHz at Max Power State with Multilayer Inductors, VDD = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x4F, 23.7 mA
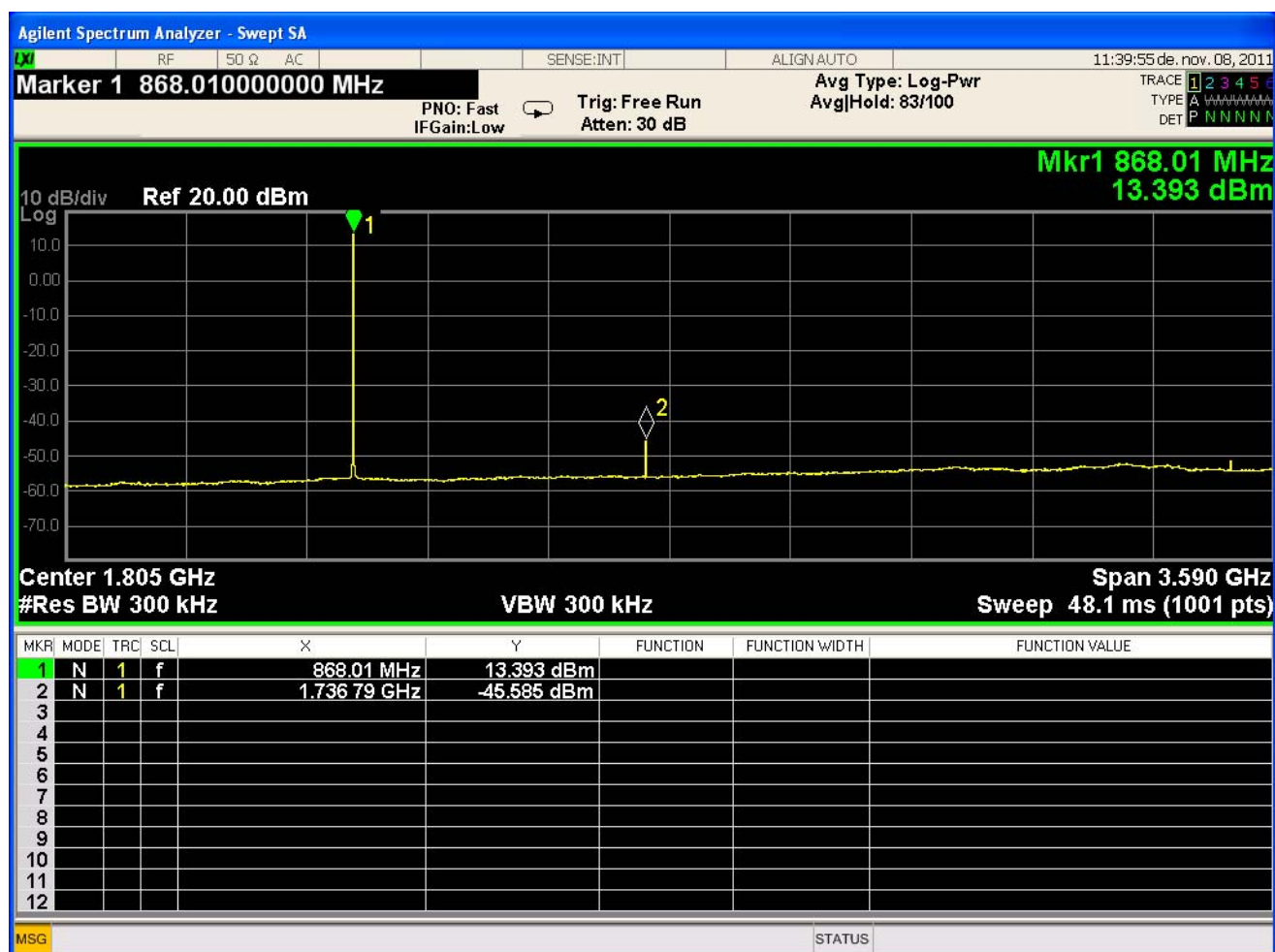
Figure 79. Si4460/67 13 dBm Direct Tie HP TX/RX Board at 868 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x3C, 24.1 mA
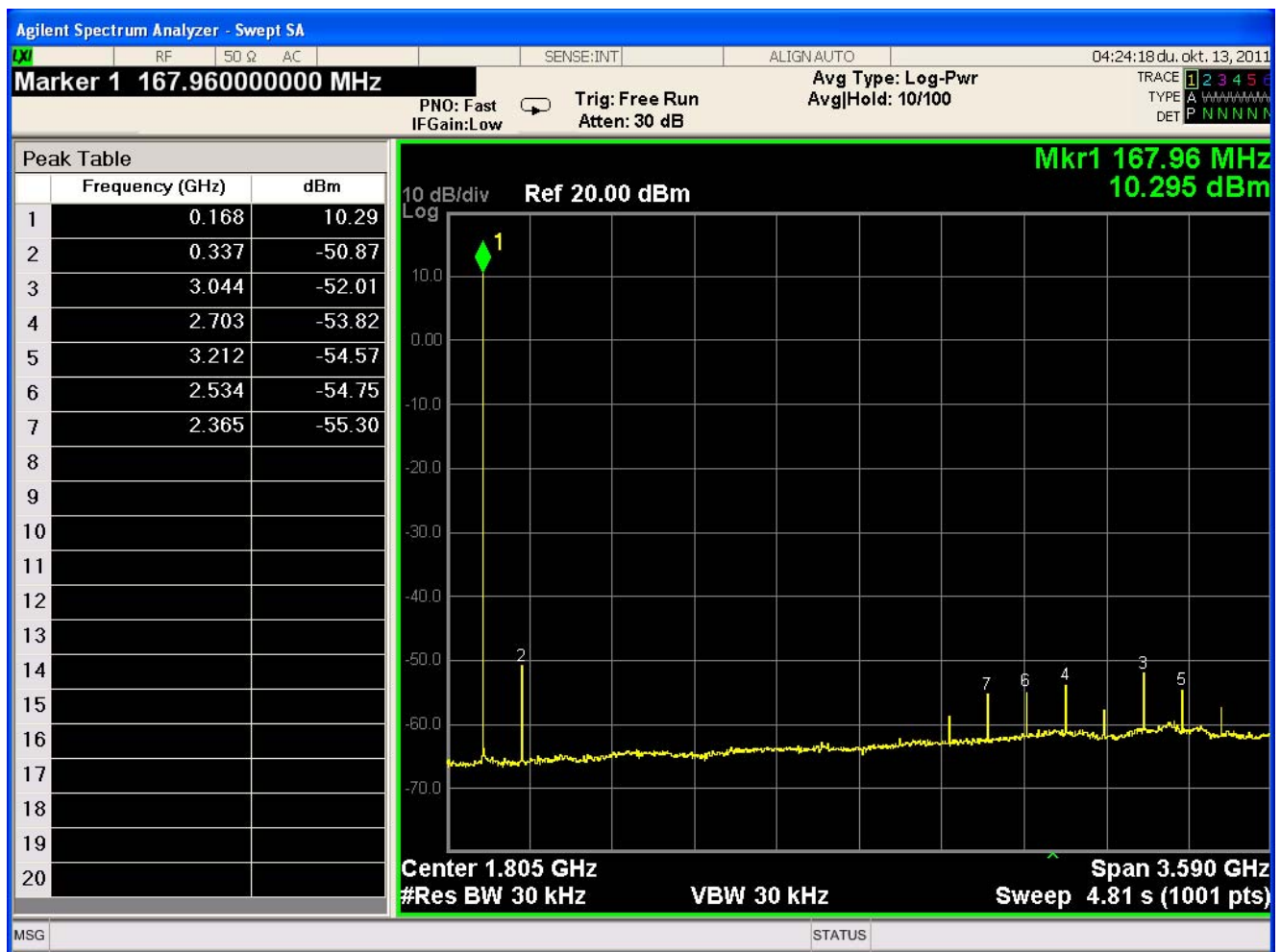
Figure 80. Si4460/67 10 dBm Direct Tie TX/RX Board at 169 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x23, 18.4 mA

AN627

Marker 1 167.960000000 MHz

Peak Table

	Frequency (GHz)	dBm
1	0.168	10.29
2	0.337	-50.87
3	3.044	-52.01
4	2.703	-53.82
5	3.212	-54.57
6	2.534	-54.75
7	2.365	-55.30

Mkr1 167.96 MHz 10.295 dBm

Center 1.805 GHz Span 3.590 GHz
#Res BW 30 kHz VBW 30 kHz Sweep 4.81 s (1001 pts)

Figure 80. Si4460/67 10 dBm Direct Tie TX/RX Board at 169 MHz with Multilayer Inductors, V_{DD} = 3.2 V, DDAC[6:0] Field in the PA_PWR_LVL Register is 0x23, 18.4 mA

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DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Revised "1. Introduction" on page 1.
- Revised "2. Summary of Matching Network Component Values" on page 6.
- Added "4. Class E (CLE) Matching Procedure Overview" on page 52.
- Added "5. CLE Matching Procedure for the Si4060/Si4460/61/67" on page 58.
- Added " Appendix A—Measured Spectrum Plots" on page 90.

Revision 0.2 to Revision 0.3

- Added " Table of Contents" on page 4.
- Extended introduction with more detailed descriptions.
- Updated "2.1.2. Si4461 with Direct Tie TX/RX SWC Board Configuration: Component Values and Performance" on page 9.
  - Added a new 868M Si4461 SWC DT Match (FC868M) with flat Pout vs. Vdd characteristic in new Tables 4 and 5 in this section.
  - Added Table 6 in this section.
- Added description of 25% duty cycle PA mode used in Si4460 Class E matches in "2.2. Component Values for Si4060/Si4460/67 and EZR32 R60/67/55 Matchings" on page 17.
- New 10 dBm Si4460 Class E 868/915M dual band DT match (old 10 dBm 868M Class E DT eliminated) given in new Tables 16, 18, and 20 (element values and measured results).
- Added Table 22, "Output Power, Current Consumption vs. Vdd (Direct Tie Si4460/67 434M CLE Board, WW Inductors)," on page 24.
- Added "2.2.3. Si4060/4460/67 with Split TX\RX SWC Board Configuration: Component Values and Performance" on page 25.
- Added "2.2.4. Si4460/67 with Direct Tie TX/RX SWC Board Configuration: Component Values and Performance" on page 25.
- New Tables 23, 24, and 25.
- Added Figure 8, "Matching Topology for Single Antenna with Direct Tie SWC Board Configuration," on page 27.
- Updated " Appendix A—Measured Spectrum Plots" on page 90.
 - Added new Figures 68–71 and 75–78.

Revision 0.3 to Revision 0.4

- Added new part (Si4467)

- Added Si4461 DT Class-E 915 MHz +16 dBm multilayer matching.
- Bug fixing.

Revision 0.4 to Revision 0.5

- Added 315/345/390 MHz + 10 dBm DT multilayer matches for Si4060/4460/4467
- Added Si4060/4460/4467 + 13 dBm matching for 863-921 MHz frequency band
- Updated filter component values for Si4060/4460/4467 + 10 dBm 868 MHz matches
- Added EZR32-related notes and matching networks.
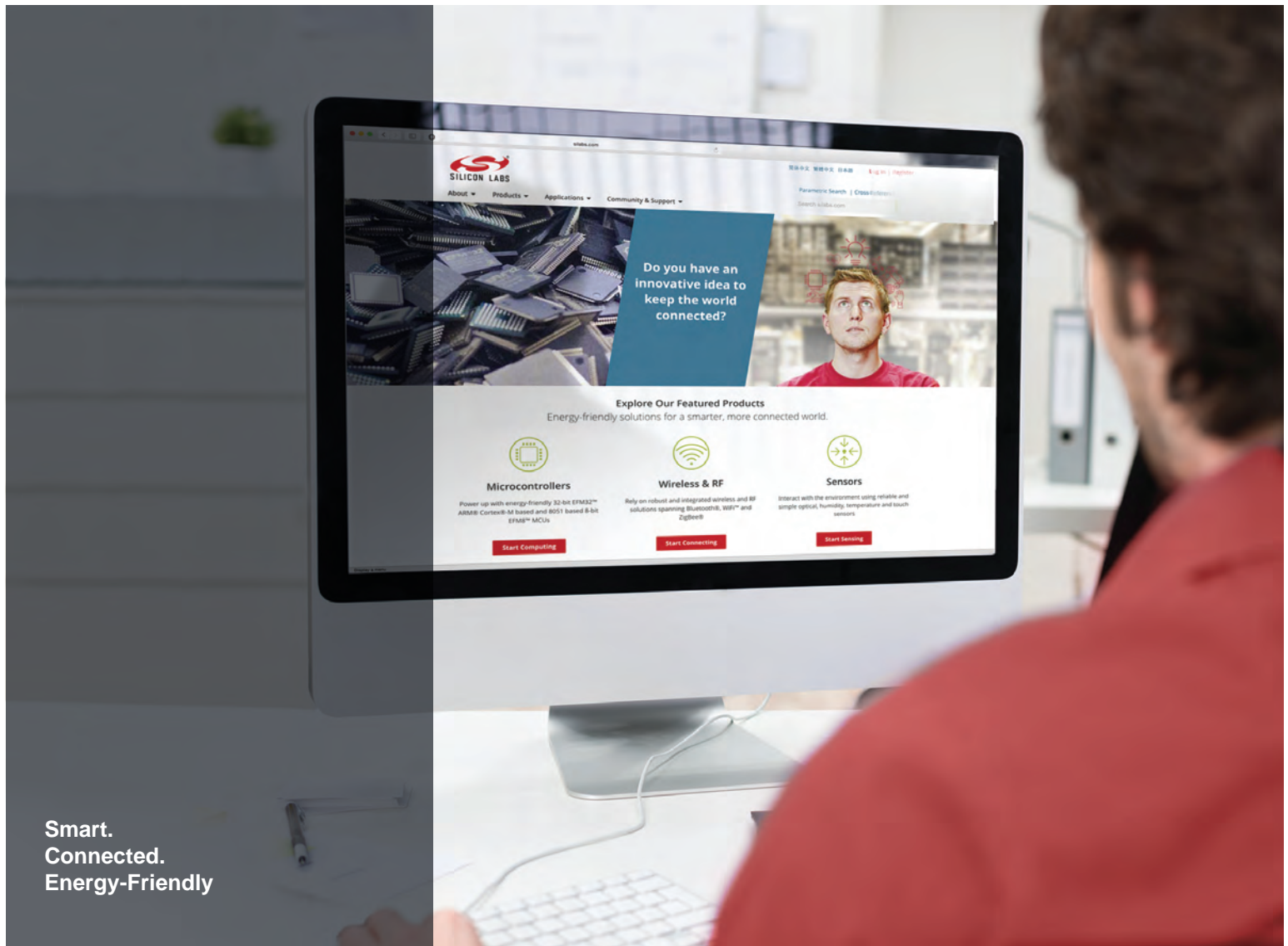
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